Asian Power Electronics Journal

PERC, HK PolyU

First edition Dec 2013 Printed in Hong Kong by Reprographic Unit
The Hong Kong Polytechnic University

Published by

Power Electronics Research Centre
The Hong Kong Polytechnic University
Hung Hom, Kowloon, Hong Kong

ISSN 1995-1051

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Improve the Performance of Intelligent PI Controller for Speed Control of SEDM using MATLAB

A. K. Singh [1] A.K. Pandey [2] M. Mehrotra [3]

Abstract–In this paper a new approach is develop for speed control of separately excited D.C. motor by enhancing the feature of artificial neural networks (ANN).The development of artificial Neural Network controller for D.C. drives is inspired by the ANN control strategy. The aim of the proposed schemes is to improve dynamic performance of separately excited D.C. motor [6]. The ANN concept is applied for both control strategy i.e. current and speed for D.C. separately excited motor. This new concept enhances the performance and dynamics of D.C. motor in comparison to conventional PI controllers and this is verified through simulation using MATLAB/SIMULINK.

Keywords–DC motor, ANN, PI controller, NARMA-L2 controller

I. Introduction

The separately excited Direct current (DC) motors with conventional Proportional Integral (PI) speed controller are generally used in industry. This can be easily implemented and are found to be highly effective if the load changes are small. However, in certain applications, like rolling mill drives or machine tools, where the system parameters vary substantially and conventional PI or PID controller is not preferable due to the fact that, the drive operates under a wide range of changing load characteristics.

The artificial neural network (ANN), often called the neural network, is the most generic form of Artificial Intelligence for emulating the human thinking process compared to the rule-based Expert system and Fuzzy Logic [2]. Multilayer neural networks have been applied in the identification and control of dynamic systems. The three typical commonly used neural network controllers: model predictive control, NARMA-L2 control, and model reference control are representative of the variety of common ways in which multilayer networks are used in control systems. As with most neural controllers, they are based on standard linear control architectures [3].There are a number of articles that use ANNs applications to identify the mathematical D.C. motor model and then this model is applied to control the motor speed [4]. They also use inverting forward ANN with input parameters for adaptive control of D.C. motor [5].

This paper address the study of steady-state and dynamics control of dc machines supplied from power converters and their integration to the load. This paper a comparative study of artificial neural networks over conventional controller such as PI speed and current controller. With the help of transfer function models, analysis of the performance of the dc motor drives for different cases has been done.

The paper first received 9 Jan 2013 and in revised form 28 July 2013.
Digital Ref: APEJ-2013-04-412

[1] Department of Electrical Engineering, M. M. M. Engineering College, Gorakhpur (U.P.), India, E-mail: er,amit0007@gmail.com
[2] Department of Electrical Engineering, M. M. M. Engineering College, Gorakhpur (U.P.), India, E-mail: akp1234@gmail.com
[3] Department of Electrical Engineering, M. M. M. Engineering College, Gorakhpur (U.P.), India, E-mail: manjari.mehrotra81@gmail.com

II. Two-Quadrant Three-Phase Converter controlled DC Motor Drive

The control schematic of a two converter controlled separately excited dc motor is shown in Fig.1. The thyristor bridge converter gets its ac supply through a three phase transformer and fast acting ac contactors. The field is separately excited, and the field supply cannot be kept constant or regulated. The DC motor has a tacho-generator whose output is utilized for closing the speed loops. The motor is driving a load considered to be frictional for this treatment. The output of the tacho-generator is filtered to remove the ripples to provide the signal, ω_{mr}. The speed command and ω_r* is compared to the speed signal to produce a speed error signal. This signal is processed through a proportional plus integrator (PI) controlled to determine the torque command. The torque command is limited, to keep it within the safe current limits. The armature current command i_a* is compared to the actual armature current i_a to have a zero current error. In case, there is an error, a PI current controller process it to alter the control signal v_c. The control signal accordingly modifies the triggering angle α to be sent to the converter for implementation [2]. The operation of closed speed controlled drive is explained from one or two particular instances of speed command. A speed from zero to rated value is commanded, and the motor is assumed to be at standstill, this will generate a large speed error and a torque command and in turn an armature current command. The armature current error will generate the triggering angle to supply a preset maximum dc voltage across the motor terminals.

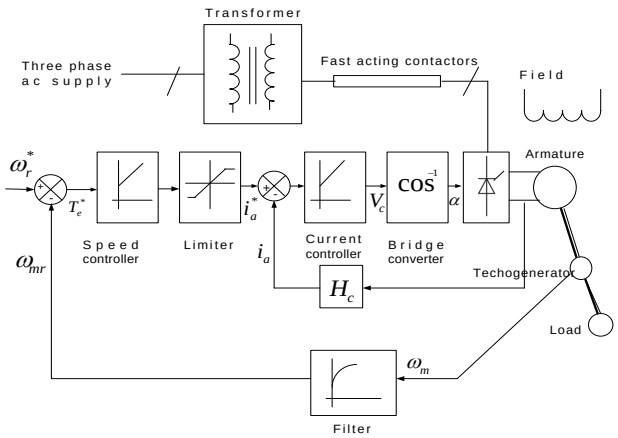

Fig.1: Speed –controlled two quadrant dc motor drive

The inner current loop will maintain the current at level permitted by its commanded value. When the rotor attains the commanded value, the torque command will settle down to a value equal to the sum of load torque and other motor losses to keep the motor in steady state. The design of the gain and time constant of the speed and current controllers is of paramount importance in meeting the dynamic specifications of the motor drives.

III. Modeling and Design of Subsystems

A. DC motor and load

The dc machine contains an inner loop due to the induced emf. It is not physically seen; it is magnetically coupled. The inner current loop will cross this back-emf loop, creating a complexity in the development of the model. The development of such a block diagram for the dc machine is shown in Fig.2. The load is assumed to be proportional to speed and is given as

$$T_l = B_l \omega_m \tag{1}$$

To decouple the inner current loop from the machine-inherent induced-emf loop, it is necessary to split the transfer function between the speed and voltage into two cascade transfer functions, first between speed and armature current and then between armature current and input voltage, represented as

$$\frac{\omega_m(s)}{V_a(s)} = \frac{\omega_m(s)}{I_a(s)} \cdot \frac{I_a(s)}{V_a(s)} \tag{2}$$

$$\frac{\omega_m(s)}{I_a(s)} = \frac{K_b}{B_t(1+sT_m)} \tag{3}$$

$$\frac{I_a(s)}{V_a(s)} = K_1 \frac{(1+sT_m)}{(1+sT_1)(1+sT_2)} \tag{4}$$

$$T_m = \frac{J}{B_t} \tag{5}$$

$$B_t = B_1 + B_l \tag{6}$$

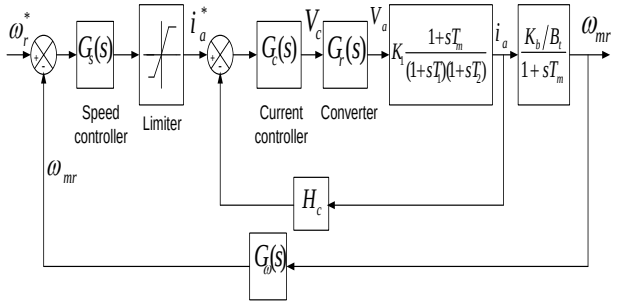

Fig.2: Block diagram of the motor drive

$$-\frac{1}{T_1}, \frac{1}{T_2} = -\frac{1}{2}\left[\frac{B_t}{J} + \frac{B_a}{L_a}\right] \pm \sqrt{\frac{1}{4}\left(\frac{B_t}{J} + \frac{B_a}{L_a}\right)^2 - \left(\frac{K_b^2 + R_a B_t}{JL_a}\right)} \tag{7}$$

$$K_1 = \frac{B_t}{K_b^2} + R_a R_t \tag{8}$$

B. Design of Controllers

The design of control loops starts from the innermost (fastest) loop and proceeds to the slowest loop, which in this case is the outer speed loop. The reason to proceed from the inner to the outer loop in the design process is that the gain and time constants of only one controller at a time are solved. Instead of solving for the gain and time constants of all the controllers simultaneously not only that is logical; it also has a practical implication. Note that every motor drive need not be speed controlled but may be torque-controlled, such as for a traction application. In that case, the current loop is essential and exists regardless of whether the speed loop is going to be closed. Additionally, the performance of the outer loop is dependent on the inner loop; therefore, the tuning of the inner loop has to precede the design and tuning of the outer loop.

a. Current Controller

The current control loop is shown in Fig.3. the loop gain function is

$$GH_i(s) = \frac{K_1 K_c K_r H_c}{T_c} \cdot \frac{(1+sT_c)(1+sT_m)}{s(1+sT_1)(1+sT_2)(1+sT_r)} \tag{9}$$

This is a fourth-order system, and simplification is necessary to synthesize a controller without resorting to a computer. Noting that T_m is on the order of a second and in the vicinity of the gain crossover frequency, we see that the following approximation is valid:

$$(1+sT_m) \cong sT_m \tag{10}$$

this reduces the loop gain function to

$$GH_i(s) = K \cdot \frac{(1+sT_c)}{(1+sT_1)(1+sT_2)(1+sT_r)} \tag{11}$$

where

$$K = \frac{K_1 K_c K_r H_c T_m}{T_c} \tag{12}$$

the time constants in the denominator are seen to have the relationship

$$T_r < T_2 < T_1 \tag{13}$$

The equation (11) can be reduced to second order, to facilitate a simple controller synthesis, by judiciously selecting

$$T_c = T_2 \tag{14}$$

Then the loop function is

$$GH_i(s) = \frac{K}{(1+sT_1)(1+sT_r)} \tag{15}$$

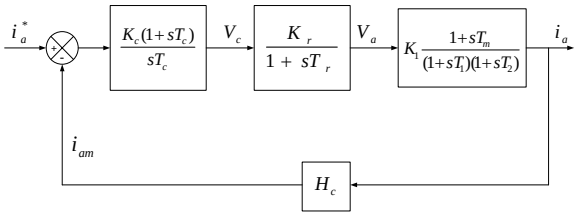

Fig. 3: Current control loop

The characteristic equation or denominator of the transfer function between the armature current and its command is

$$(1+sT_1)(1+sT_r)+K \tag{16}$$

this equation is expressed in standard form as

$$T_1T_r\left\{s^2+s\left(\frac{T_1+T_2}{T_1T_r}\right)+\frac{K+1}{T_1T_r}\right\} \tag{17}$$

From which the neural frequency and damping ratio are obtained as

$$\omega_n^2 = \frac{K+1}{T_1T_r} \tag{18}$$

$$\varsigma = \frac{\frac{T_1+T_r}{T_1T_r}}{2\sqrt{\frac{K+1}{T_1T_r}}} \tag{19}$$

where ω_n and ς are the natural frequency and damping ratio, respectively. For good dynamic performance, it is an accepted practice to have a damping of 0.707.Hence, equating the damping ratio to 0.707 in equation (19), we get

$$K+1 = \frac{\left(\frac{T_1+T_r}{T_1T_r}\right)^2}{\frac{2}{T_1T_r}} \tag{20}$$

Realizing that

$$K \gg 1 \tag{21}$$

$$T_1 \gg T_r \tag{22}$$

Tells us that K is approximated as

$$K \cong \frac{T_1^2}{2T_1T_r} \cong \frac{T_1}{2T_r} \tag{23}$$

by equating equation (12) to (23).the current-controller gain is evaluated

$$K_c = \frac{1}{2}\frac{T_1T_c}{T_r}\left(\frac{1}{K_1K_rH_cT_m}\right) \tag{24}$$

b. Speed Controller

The speed loop with the first-order approximation of the current-control loop is shown in Fig.4.The loop gain function is

$$GH_s(s) = \frac{K_sK_iK_bH_w}{B_tT_s}\cdot\frac{(1+sT_s)}{s(1+sT_1)(1+sT_m)(1+sT_\omega)} \tag{25}$$

This is a fourth-order system. To reduce the order of the system for analytical design of the speed controller, approximation serves. In the vicinity of the gain crossover frequency, the following is valid

$$(1+sT_m) = sT_m \tag{26}$$

The next approximation is to build the equivalent time delay of the speed feedback filter and current loop. Their sum is very much less than the integrator time constant T_s and hence the equivalent time delay, T_4 can be considered the sum of the two delays, T_i and $T\omega$. This step is very similar to the equivalent time delay introduced in the simplification of the current loop transfer function.Hence, the approximate gain function of the speed loop is

$$GH_s(s) \cong K_2\frac{K_s}{T_s}\frac{(1+sT_s)}{s^2(1+sT_4)} \tag{27}$$

where

$$T_4 = T_i + T_\omega \tag{28}$$

$$K_2 = \frac{K_iK_bH_\omega}{B_tT_m} \tag{29}$$

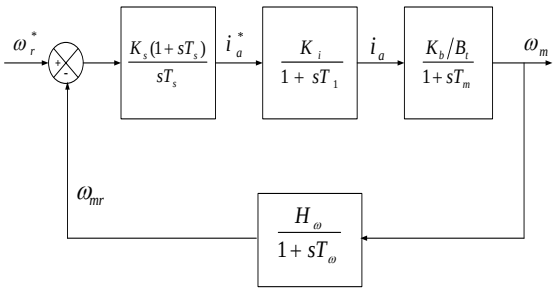

Fig.4: Representation of the outer speed loop in the dc motor drive

The closed loop transfer function of speed to its command is

$$\frac{\omega_m(s)}{\omega_r^*(s)} = \frac{1}{H_\omega}\left[\frac{\frac{K_2K_s}{T_s}(1+sT_s)}{s^3T_4+s^2K_2K_s+\frac{K_2K_2}{T_s}}\right] = \frac{1}{H_\omega}\frac{(a_0+a_1)}{(a_0+a_1s+a_2s^2+a_3s^3)} \tag{30}$$

where

$$a_0 = K_2K_s/T_s \tag{31}$$

$$a_2 = K_2 K_s \tag{32}$$

$$a_2 = 1 \tag{33}$$

$$a_3 = T_4 \tag{34}$$

This transfer function is optimized to have a wider bandwidth and a magnitude of one over a wide frequency range by looking at its frequency response. Its magnitude is given by

$$\left|\frac{\omega_m(j\omega)}{\omega_r^*(j\omega)}\right| = \frac{1}{H_\omega}\sqrt{\frac{a_0^2+\omega^2 a_1^2}{\{a_0^2+\omega^2(a_1^2-2a_0a_2)+\omega^4(a_2^2-2a_1a_3+\omega^6 a_3^2)+\omega^6 a_3^2\}}} \tag{35}$$

This is optimized by making the coefficients ω^2 and ω^4 equal to zero, to yield the following conditions

$$a_1^2 = 2a_0a_2 \tag{36}$$

$$a_2^2 = 2a_1a_3 \tag{37}$$

Substituting these conditions in terms of the motor and controller parameters given in (31) into (34) yields

$$T_s^2 = \frac{2T_s}{K_s K_2} \tag{38}$$

Resulting in

$$T_s K_s = \frac{2}{K_2} \tag{39}$$

Similarly

$$\frac{T_s^2 s}{K_s^2 K_2^2} = \frac{2T_s^2 T_4}{K_s K_2} \tag{40}$$

Thus after simplification, gives the speed – controller gain as

$$K_s = \frac{1}{2K_2T_4} \tag{41}$$

Substituting equation (41) into equation (39) gives the time constant of the speed controller as

$$T_s = 4T_4 \tag{42}$$

Substituting for K_s and T_s into equation (38) gives the closed-loop transfer function of the speed to its command as

$$\frac{\omega_m(s)}{\omega_m^*(s)} = \frac{1}{H_\omega}\left[\frac{1+4T_4 s}{1+4T_4 s+8T_4^2 s^2+8T_4^2 s^2+8T_4^3 s^3}\right] \tag{43}$$

It is easy to prove that for the open-loop gain function the corner points are$1/4T_4$ and $1/T_4$, with the gain crossover frequency being $1/2T_4$.

IV. NARMA-L2 CONTROL

The central idea of this type of control is to transform nonlinear system dynamics into linear dynamics by canceling the nonlinearities. This section begins by presenting the companion form system model and demonstrating how you can use a neural network to identify this model [11]. Then it describes how the identified neural network model can be used to develop a controller. The tapped delay line (TDL), to make full use of the linear network. There the input signals enter from the left and passes through N-1 delays. The output of the tapped delay line (TDL) is an N-dimensional vector, made up of the input signal at the current time, the previous input signal. Using the NARMA-L2 model, you can obtain the controller.

$$u(k+1) = \frac{y_r(k+d) - f[y(k),\cdots,y(k-n+1),u(k),\cdots,u(k-n+1)}{g\left[y(k),\cdots,y(k-n+1),u(k),\cdots,u(k-m+1)\right]} \tag{44}$$

which is realizable for $d \geq 2$.

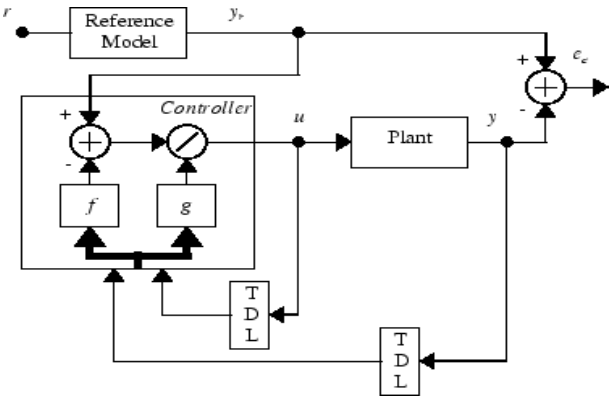

Fig.5: Block diagram of the NARMA-L2 controller

This controller can be implemented with the identified NARMA-L2 plant model, as shown in the Fig.6.

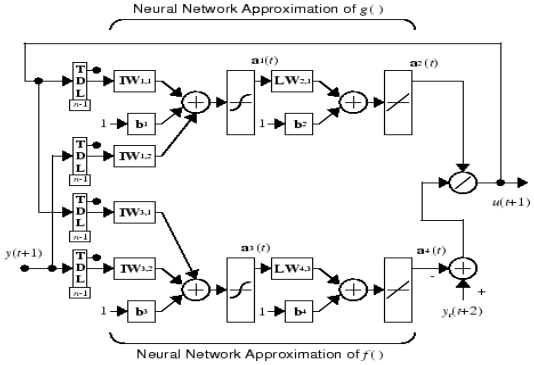

Fig. 6: Identified NARMA-L2 plant model

V. SIMULINK MODEL AND RESULTS

A. Response of the system using current and speed control strategy with conventional PI controller

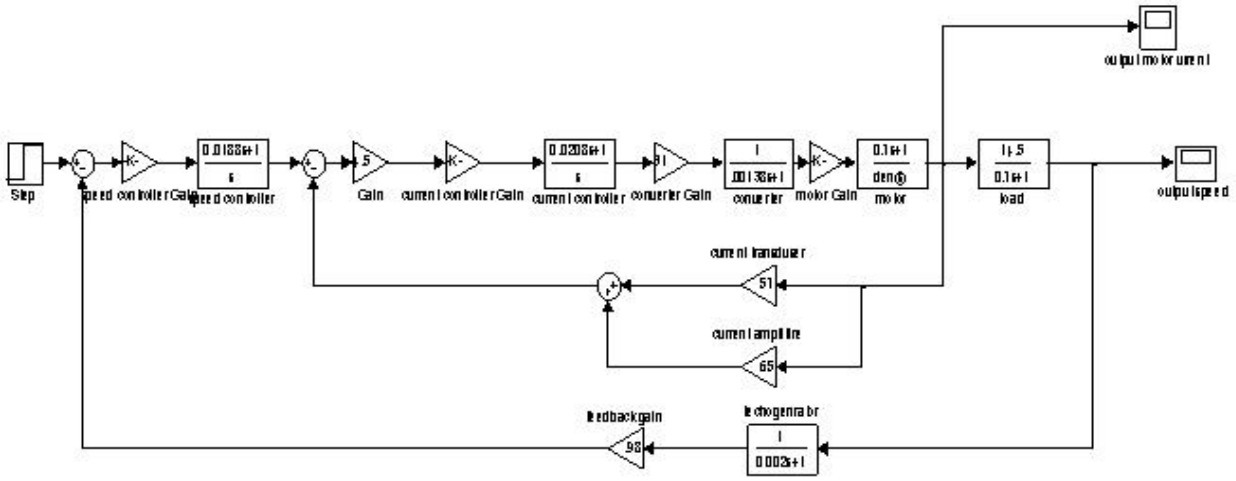

Fig.7: Simulink plant model with speed and current controller

In this control strategy, current control and speed control are applying for improving the performance of DC motor drive. In Fig.7.Shows the simulation plant model for this case. The responses are shown in Fig.8(a) and 8(b).

B. Control strategy with ANN controller (NARMA-L2 CONTROL)

In this text consider the simulink modeling of a separately excited DC motor with speed and current controller using ANN. The entire conventional PI controller is replaced by ANN. The control system of DC motor using neural networks is presented. In this case study where use the either single neural network as a controller for the control the speed of DC drive with using Both control strategy. The performance of DC motor drive with ANN controller is evaluated by simulink plant model. The plant input and output data are generated by neural network tools of MATLAB/SIMULINK for training of neural networks. The control signal for converters according to plant output is generated by trained ANN on the basis of plant identification. In this study use the different type of cases are as follows:

a. Using only current controller
b. Using only speed controller
c. Single ANN controller with both current and speed control

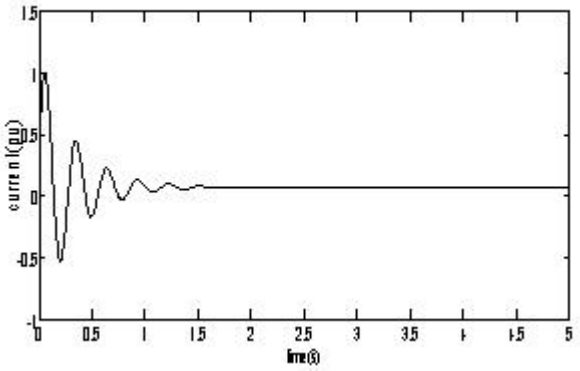

Fig.8 (a): Output motor current response

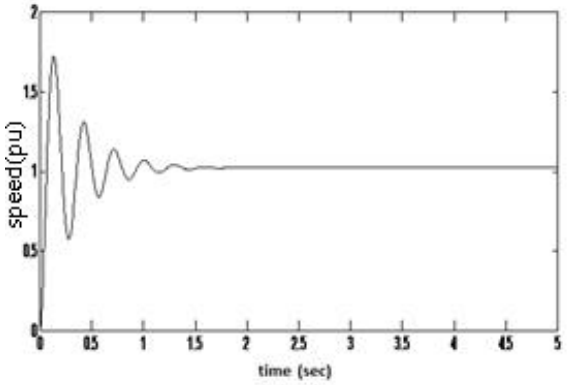

Fig.8 (b): Output motor speed response

a. Response of system using only current control strategy with ANN:

In this case reference plant have only current controller, shown in Fig.10.The input and output data are generated by this reference plant which is shown in Fig.12.The complete plant layout is given in Fig.9.The neural network specification are shown in Fig.11.The response of the system with simulink plant model with ANN, using current control strategy is shown in Fig.13.The result shows that the response of the system is better than using conventional PI controller.

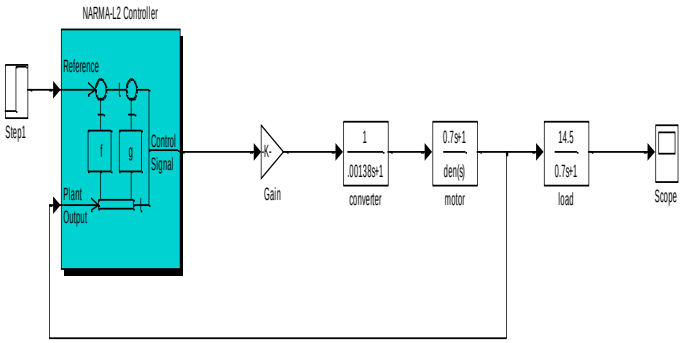

Fig.9: Simulink plant model using only current control strategy with ANN

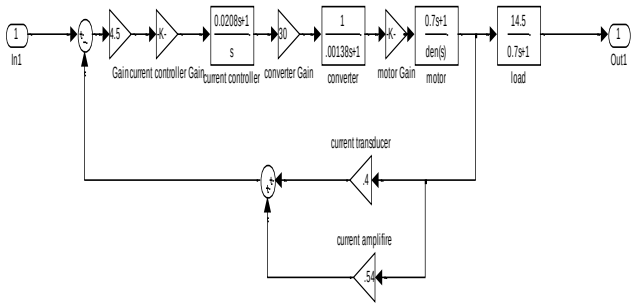

Fig.10: Simulink reference plant model for training of ANN with current controller

b. Response of the system using only speed control strategy with ANN:

In this case plant layout is shown in Fig.14. Only change the plant specification of ANN and reference plant model which is shown in Fig.15&16. The input and output data are generated by this reference plant which is shown in Fig.17.The response of the system with simulink plant model with ANN, using speed control strategy is shown in Fig.18.The results show that the response of the system is not so poor but the settling time is more in comparison to (a).

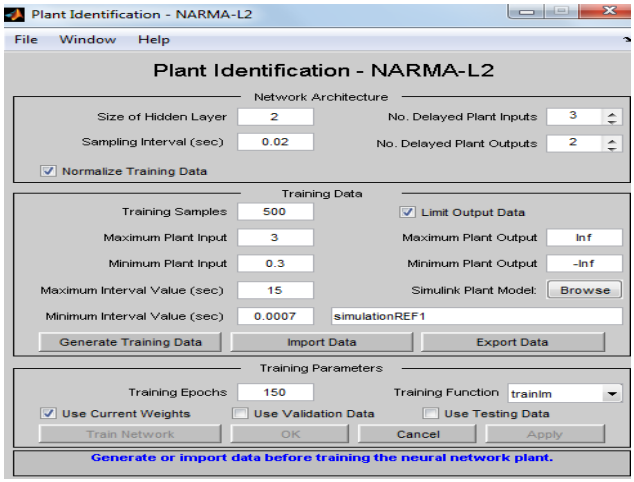

Fig.11: ANN and Plant specification model with only current control strategy

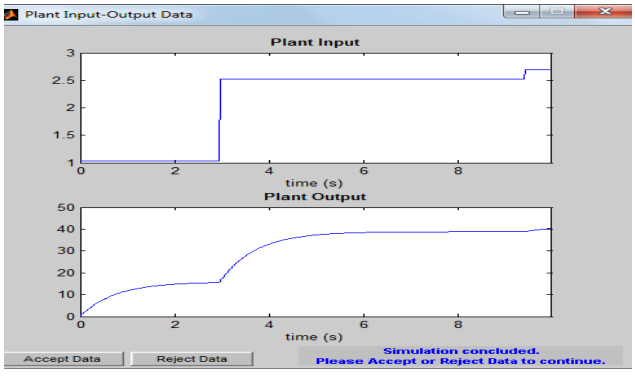

Fig.12: Plant input and output generated by reference plant for ANN

c. Response of system using speed and current control with ANN:

In this case only single neural network is used for both speed and current control strategy which is shown in Fig.19. Reference model for training of ANN with current and speed controller is shown in Fig.20. The plant specification and plant input output model with both current and speed control strategy is shown in Fig.21 and 22. The response of the system is shown in Fig.23. The result of this system shows that the response of the plant is so better in comparison to previous cases as well as conventional PI control methods.

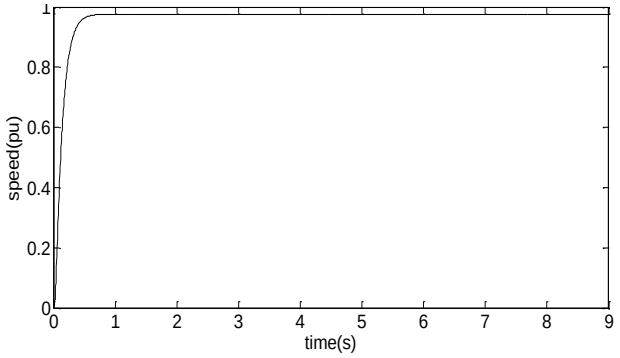

Fig.13: Plant output with current control strategy using ANN as current controller

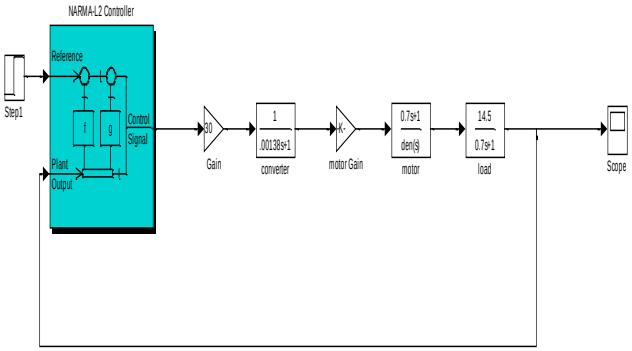

Fig.14: Simulink plant model using only speed control strategy with ANN

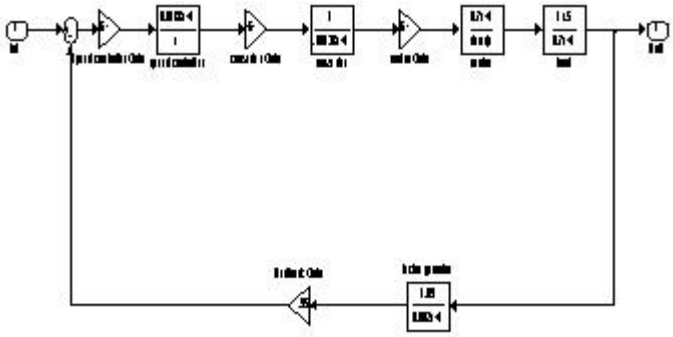

Fig.15: Simulink reference model for training of ANN with speed controller

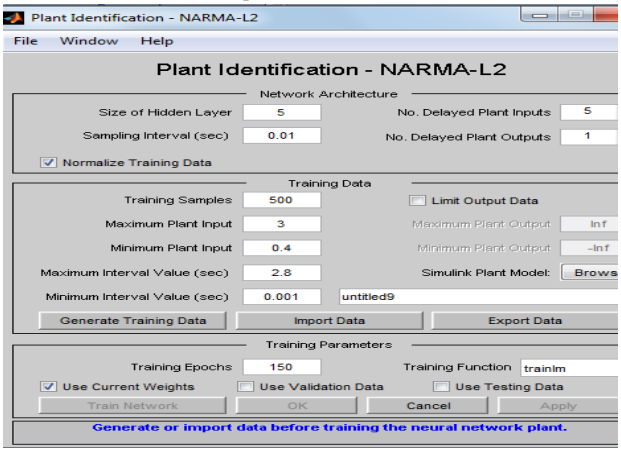

Fig.16: ANN and plant specification model with only speed control strategy

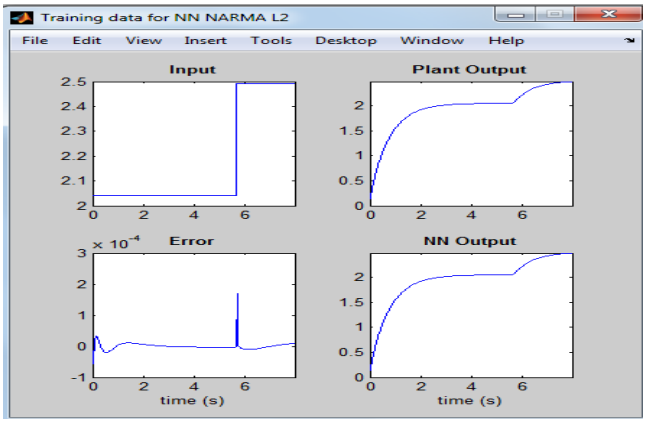

Fig.17: Plant input and output generated by reference plant for ANN

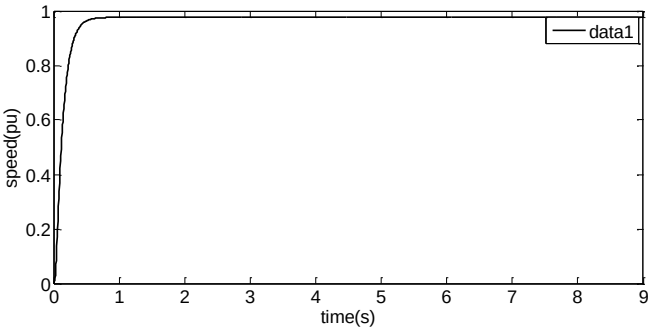

Fig.18: Plant output speed control strategy using ANN as speed controller

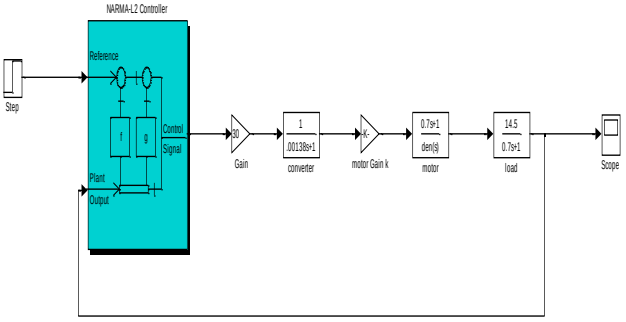

Fig.19: Simulink plant model with current and speed control using ANN

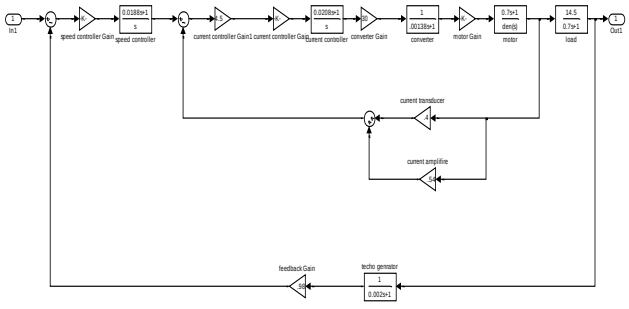

Fig.20: Simulink reference model for training of ANN with current and speed controller both

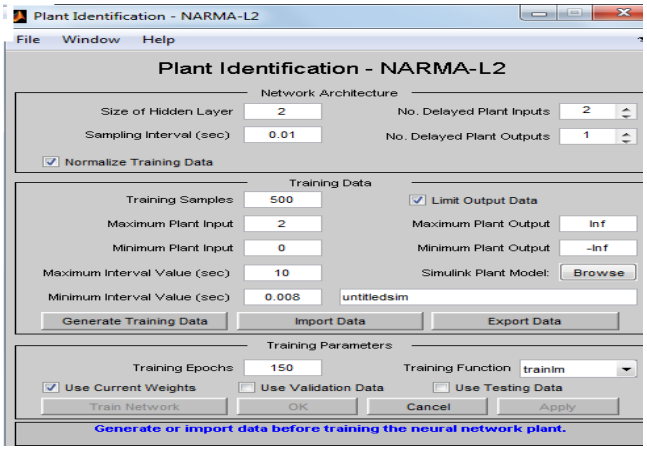

Fig.21: ANN and plant specification model with current and speed control strategy

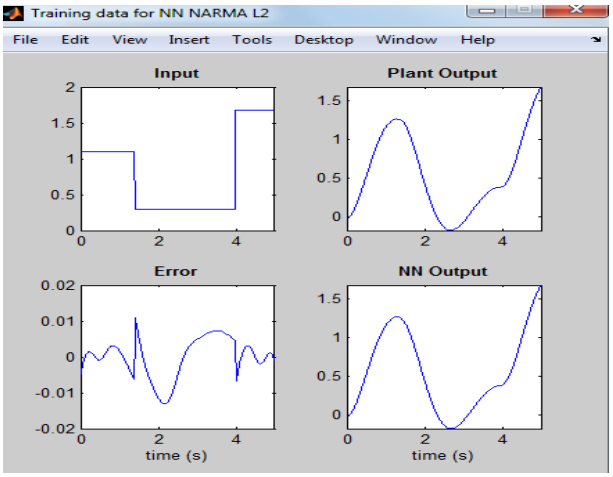

Fig.22: Plant input, output and ANN training error

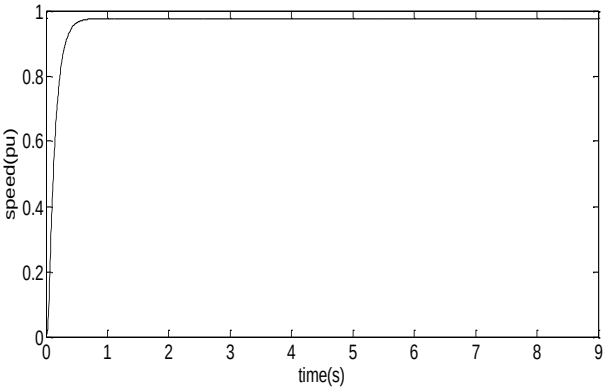

Fig.23: Plant output with current and speed control strategy using single ANN

VI. Results and Discussion

In this work actually evaluated the performance of a dc motor with a constant load using different type of control strategy conventional (PI) and modern (ANN) controller concept. Using the ANN controller concept with dc motor the performance and dynamics of the dc motor is improved in comparison to the conventional PI controllers. The simulation of the complete drive system is carried out based on training for different reference plant with different control strategy. The D.C. motor has been successfully controlled using an ANN. Firstly, one ANN

controller is used with only Current control strategy. The results with both speed and current control strategy are better as compared to the results obtained with only current control and speed control strategy. The simulation result (Fig.23) shows that the response of the plant with both current and speed controller is better as compared to conventional methods (Table 1). The results prove that the complete D.C. drive system is robust to parameter variations. All the comparisons for the different cases are tabulated in Table 1.

Table 1: speed response

Cases		Settling time t_s (sec.)	Maximum overshoot (mp) p.u.	Steady state error (p.u.)
(A) Conventional control (PI)	For speed	1.8	1.7	0.02
	For current	1.7	1.0	0.03
(B) Modern control (ANN)	I	0.85	No overshoot	0.03
	II	0.95	No overshoot	0.04
	III	0.74	No overshoot	0.02

VII. Conclusion

By using ANN mode controller for the separately excited DC motor speed control, the following advantages have been realized.

The speed response for constant load torque shows the ability of the drive to instantaneously reject the perturbation. The design of controller is highly simplified by using a cascade structure for independent control of flux and torque. By using ANN don't have to calculate the parameters of the motor when designing the system control. By using ANN the complete D.C. drive system is robust to parameters variations. The dynamic and steady state performance of the ANN based control drive is much better than the PI controlled drives. Settling time has been reduced to a label of 0.0.74 sec.

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Appendix

The following motor parameters and ratings are used for designing speed-controlled dc motor drives, maintaining the field flux constant.

Power rating = 5*HP*,
D.C. motor input voltage = 220*V*,
Armature current rating = 8.2*A*,
Rated speed = 1470 rpm,
Armature resistance *Ra* = 4 *Ω*,
Moment of inertia $J = 0.0609\ kg\text{-}m^2$,
Armature Inductance *La* = 0.074*H*,
Viscous friction coefficient *Bt* = 0.0867 *Nms/rad*,
Torque constant *Kb* = 1.23 *V/rad/s*.
Converter Supplied voltage = 230 *V*,
3 – Phase, A.C. Frequency = 50 *Hz*,
Maximum control input voltage is ± 10 *V*.
Maximum current permitted in the motor is 20 *A*.
Number of training sample is 500.
Number of training epoche is 150
Number of hidden layers is 2.

Biographies

Amit Kumar Singh received his M.tech degree in Power Electronics and Drives from M.M.M. Engineering College, Gorakhpur, (U.P) in 2012. He did his B.Tech in Electrical Engineering from R.G.E.C Meerut in 2009. Currently he is working as Assistant Professor in Electrical and Electronics Department in SCERT Barabanki, (U.P.). His areas of current interest include electrical machines, control

systems, power electronics and electric drives.

Ashok Kumar Pandey received his Ph.D. degree in Electrical Engineering from Indian Institute of Technology, Roorkee in 2003. He did his M.Tech. in Power Electronics, Electrical Machines and Drives from Indian Institute of Technology, Delhi in 1995. Currently, he is working as an Associate Professor with the Department of Electrical Engineering at M.M.M. Engineering College, Gorakhpur, (U.P.), India. His areas of interest include power electronics, electrical machines, and drive.

Manjari Mehrotra received his M.Tech degree in Power Electronics and Drives from M.M.M. Engineering College, Gorakhpur, (U.P) in 2012. She obtained her B.Tech degree in Electrical Engineering from R.G.E.C Meerut in 2009. Currently she is working as Assistant Professor in Electrical and Electronics Department in SCERT Barabanki, (U.P.). Her areas of current interest include electrical machines, power electronics and electric drives.

Control Strategy with Game Theoretic Approach in DC Micro-grid

Mingxuan Wu [1] Lei Dong [2] Furong Xiao [3] Xiaozhong Liao[4]

Abstract–This paper proposes a decentralized control algorithm for DC micro-grid which is based on the game theory without communication, the proposed algorithm is an application of the Nash certainty equivalence principle. Since it is achieved without communication, it benefits from concerned reliability issues. Compared with the droop control system, extensive analysis based on simulations demonstrates that the proposed modeling, although simplified, is sufficient for an adequate control system design. The proposed control algorithm brings more accurate DC bus voltage and good current sharing performance. The simulation results verify the voltage stability and accuracy of DC bus, and current-sharing control of DC-DC converters are achieved simultaneously.

Keywords–Nash certainty equivalence principle, DC Micro-grid, game theory, distribute generation

I. INTRODUCTION

Nowadays, energy and environmental problems are interrelated with the factors, such as the growth of energy demand, and the high quality with safe and reliable electric requirement. Against the background of these problems, a large number of distributed generations (DGs) are being installed into power systems. However, it is well known that an insertion of many DGs affects power quality of the utility grids, and it may cause problems such as rising of voltage and protection problem. In order to solve these problems, one of the solutions is to construct a new power system, i.e. micro-grids which have been especially researched all over the world [1]. DC distribution micro-grids are suitable for those kinds of energy storages and DGs, which can reduce conversion losses and supply high quality power [2]. There are some advantages using DC micro-grid in practice [3].

In the literature, most control strategies depend on a communication infrastructure. Reference [4] presents the operation of a multi-agent system for the control of a micro-grid. The expensive communication system can be avoided by using active power/frequency droop control in the conventional grid control system [6,7]. An improved droop control principle is presented for the control of generators in an islanded micro-grid [8]. The droop control method is a good solution for load sharing. However, the conventional droop method also has several drawbacks including a slow transient response, a trade-off between load sharing accuracy and voltage deviation [12]. The load sharing accuracy is affected by line, DG output impedances and corresponding voltage drops. To improve the accuracy of load sharing, increased droop gain scheme is adopted. However, increased droop gain has a negative impact on the overall system stability. Moreover, it increases the range of system voltage variations [13-15].

In this paper, a control strategy is proposed based on the game theory which does not depend on communication infrastructure. As is shown in the Fig. 1, the multiple DG system is modeled and employs game theory [9] to design control strategy. The control strategy can minimize output voltage error. It is found that performance of each DG is practically independent in the system.

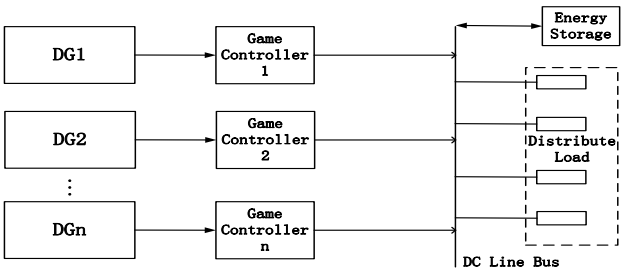

Fig.1: Multi-circuit system without communication

II. DECENTRALIZED CHARGING CONTROL PROBLEMS FOR PCS IN MICRO-GRID

The decentralized DGs charging control problem is a form of non-cooperative game, where a large number of selfish DGs transfer the electricity resources to the DC line bus to ensure the DC bus voltage stable. This paper presents a novel control strategy that achieves Nash equilibrium by simultaneously updating each DG's best individual strategy with respect to minimize the cost function. The algorithm is unrelated to the number of DGs, since they update their control strategy simultaneously and independently. The proposed decentralized charging control strategy drives the system asymptotically to a unique Nash equilibrium.

The proposed algorithm is an application of the so-called Nash certainty equivalence principle. The control algorithm can achieve optimality of the micro-grid, i.e. it can make the DC bus voltage stable and load sharing. Nash equilibrium is the most important concept in game theory. In fact, Nash equilibrium is a kind of "stalemate" in which no one is interested in changing [16].

Definition 1**:** A collection of control strategies $\{d_n^*; n \in N\}$ is Nash equilibrium if each individual DG can benefit nothing by changing its own strategy

$$J_n(d_n^*; d_{-n}^*) \le J_n(d_n; d_{-n}^*) \quad (1)$$

for all $d_n \in (0,1)$, and all $n \in N$.

The paper first received 18 Dec 2012 and in revised form 13 Mar 2013 .
Digital Ref: APEJ-2013-04-416
[1,2,3,4] School of Automation, Beijing Institute of Technology, Beijing,
[1] E-mail: wweiy1296@163.com, corresponding author
[2] E-mail: leidong@bit.edu.cn
[3] E-mail: xfrongok@126.com
[4] E-mail: liaoxiaozhong@bit.edu.cn

where d_{-n}^* is the collection of control strategies of the whole DGs without DG n [19].

In other words, d_n^* is the solution of minimum cost function

$$d_n^* \in \arg\min J_n(d_1^*,\cdots,d_{n-1}^*,d_n^*,d_{n+1}^*,\cdots,d_N^*), \quad n=1,2,\cdots,N. \tag{2}$$

Therefore, d_n^* is the control strategy which can obtain the minimum value of cost function $J_n(d_n)$.

If the two above-mentioned conditions are achieved by each DG, the micro-grid will achieve the state of Nash equilibrium, i.e. the DC micro-grid will keep voltage stable and load sharing.

A. Virtual Rivals Strategy

Assuming there are $n+1$ DGs supply power for the micro-grid which means there are n rivals for every DG. Estimation of supply power strategy for every rival will be difficult to calculate because the workload is extremely large. In this paper, a conception of virtual rivals is introduced which means to take the other DGs as an equivalent virtual rival. This will simplify the estimation for every rival and it has advantages as follows: 1) Simplicity: Reducing the number of rivals from n to 1 simplifies the model and the complexity of calculation greatly, and 2) High estimating accuracy: Estimating supply power strategy for n rivals, since the uncertainty is too much for every rival, so the estimating error is relatively large [5]. When estimating the equivalent rival, the randomness will be offset and the estimating accuracy is enhanced.

By this way, the method simplifies the n-player-game problem to two-player-game problem that simplifies the complexity of problem greatly. Therefore, in the discussion of this paper, we only discuss the two-player-game problem because it has the same result of n-player-game problem.

B. Proposed Optimal Controller

The underlying decentralized DGs charging control is a non-cooperative dynamic game. Each DG shares other DGs with the information by DC line bus voltage. So we need formulate the decentralized DGs charging control problem as a dynamic games.

We consider charging control of each DG of size M with the charging time $t=\{0,1,\cdots,T-1,T,T+1,\cdots,\infty\}$ where T denotes the ultimate charging steadily instant. The serial number of DG is denoted as $M=\{0,1,\cdots,n,\cdots,N\}$. With a control strategy of micro-grid with game theoretic approach, we assume that DGs achieve Nash equivalence at time T. The objective is to implement a collection of DGs charging strategy that achieves dual objectives, 1) the DC line bus voltage achieves setting value of voltage, and 2) each DG achieve the state of current sharing.

The objective of the control is to minimize the output voltage error. Hence, a definition of the cost function of each DG n is given by

$$\begin{aligned} J_n(u,i) &= AP + B\sum_{m=0}^{m=t-1}(k_1u_r - k_2u_m - k_3i_m)^2 + D(u_r-u_t)^2 \\ &= Au_ti_t + B\sum_{m=0}^{m=t-1}(k_1u_r - k_2u_m - k_3i_m)^2 + D(u_r-u_t)^2 \end{aligned} \tag{3}$$

where, A, B, D, k_1, k_2 and k_3 are all non-negative constant, P represents the output power of the each DG, u and i denote the output voltage and current of the each PC, u_r is the voltage reference of the DC line bus.

As is shown in (3), the output current, voltage and error of the system voltage output are included in the cost function. Where AP denotes the output power, which has the minimization of the input to the system results in minimum input energy (minimum cost). Where $B\sum_{m=0}^{m=t-1}(k_1u_r - k_2u_m - k_3i_m)^2$ determines the penalty for deviating from the setting value, and $D(u_r-u_t)^2$ denotes minimization of the output error that is one of the main targets of the system. It will be shown that the presence of the squared deviation term ensures convergence to a unique collection of locally optimal strategies which is Nash equilibrium [11]. The cost incurred in deviating from the voltage reference of the DC line bus.

This paper proposes a control scenario which individual DG minimize its own operating cost function (3). In order to minimize its own operating cost, it is adopted by calculate method of the extreme value of binary function [10].

Therefore, we can demonstrate using the control law (4) and (5) can minimize its cost function (3). The control law can be simplified as:

$$i_r = \frac{2Bk_2}{A}\sum_{m=0}^{m=t-1}(k_1u_r - k_2u_m - k_3i_m) + 2D(u_r-u_t) \tag{4}$$

and

$$k_1 = k_2 + k_3\frac{i}{u_r}. \tag{5}$$

According to the transformation in (4) and (5), through the voltage reference u_r, the previous voltage u_m and current i_m $(m=0,1,\cdots,t-1)$ and present voltage u_t can calculate the reference current i_r which can be obtained, and then detect the output current i. Finally, PI adjust is adopted for a current closed loop to ensure a suitable power output. The local information such as output voltage u and output current i can be detected directly. It is obviously that only local information can minimize the cost function. Accordingly, using this method can achieve desired performance in voltage regulation and current sharing

among the DGs. Such a structure has notable advantages such as simplicity and reliability. And this method can satisfy the most important characteristics of the micro-grid, i.e. plug and play. DG can be considered as different agents. Assuming each agent is 'rational' which means every agent always following the maximum of its own benefit function. Finally, the micro-grid system achieves the state of Nash equilibrium.

III. Small-Signal Model of Game Theoretic Strategy

A linear model is necessary for designing linear controls. An average model is sufficient for the bandwidth requirements of typical applications [17]. Accordingly, a simple average model for the buck converter is developed based on ideal transform concepts for switching. The DG's converter shown in Fig. 3 can be replaced by an average model.

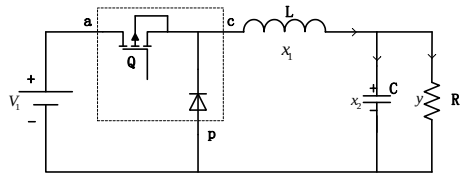

Fig. 3: The module of buck converter

At time $t=[0,d]T$, the switch Q is turned on,

$$\begin{cases} i_a(t)=i_c(t) \\ u_{cp}(t)=u_{ap}(t) \end{cases} \tag{6}$$

where d is the duty cycle of the switch Q, i_a is the input current of terminal a, i_c is the output current of terminal c. u_{cp} and u_{ap} is the voltage between terminals a, p and c respectively.

At time $t=[d,1]T$, the switch Q is turned off,

$$\begin{cases} i_a(t)=0 \\ u_{cp}(t)=0. \end{cases} \tag{7}$$

Ideal transformer averaging concepts can be directly applied to buck converter. A large signal average model can be formed with transformers by realizing (6) and (7) and similar average current equations,

$$\begin{cases} \overline{i}_a(t)=\overline{i}_c(t)\times d \\ \overline{u}_{cp}(t)=\overline{u}_{ap}(t)\times d. \end{cases} \tag{8}$$

The small signal model is formed from the large signal model by perturbing the large signal parameters about a particular operating point:

$$d=D+\hat{d},\quad \overline{u}_{cp}(t)=V_{cp}+\hat{u}_{cp},\quad \overline{u}_{ap}(t)=V_{ap}+\hat{u}_{ap},$$
$$\overline{i}_a(t)=I_a+\hat{i}_a,\quad \overline{i}_c(t)=I_c+\hat{i}_c,$$

where the set $\{D,V_{ap},V_{cp},I_a,I_c\}$ defines a particular operating point, and the set $\{\hat{d},\hat{u}_{ap},\hat{u}_{cp},\hat{i}_a,\hat{i}_c\}$ defines perturbing. The nonlinear model for the converter operating in the continuous conduction mode is given by

$$\begin{cases} I_a+\hat{i}_a=(I_c+\hat{i}_c)\times(D+\hat{d}) \\ V_{cp}+\hat{u}_{cp}=(V_{ap}+\hat{u}_{ap})\times(D+\hat{d}). \end{cases} \tag{9}$$

The dynamic model given in (9) is nonlinear and cannot be directly employed to design a control system with the most commonly used techniques, which require a linear model. However, if the magnitudes of the perturbations are much smaller than their steady-state values, the nonlinear terms can be ignored without resulting in significant error, and a linear approximation of the system is obtained. Assuming dynamic components are much smaller than steady-state components,

$$\frac{\hat{d}}{D}<<1,\frac{\hat{u}_{ap}}{V_{ap}}<<1,\frac{\hat{u}_{cp}}{V_{cp}}<<1,\frac{\hat{i}_a}{I_a}<<1,\frac{\hat{i}_c}{I_c}<<1. \tag{10}$$

So the infinitesimal of higher order $\hat{i}_c\times\hat{d}$ and $\hat{u}_{ap}\times\hat{d}$ can be neglected. Hence, (10) can be divided into steady-state component and perturbing component respectively.

Steady-state components

$$\begin{cases} I_a=I_c\times D \\ V_{cp}=V_{ap}\times D. \end{cases} \tag{11}$$

Perturbing component

$$\begin{cases} \hat{i}_a=i_c\times D+I_c\times\hat{d} \\ \hat{u}_{cp}=\hat{u}_{ap}\times D+V_{ap}\times\hat{d}. \end{cases} \tag{12}$$

Thus, a small-signal reduced-order linear model for the buck converter can be defined as Fig. 4.

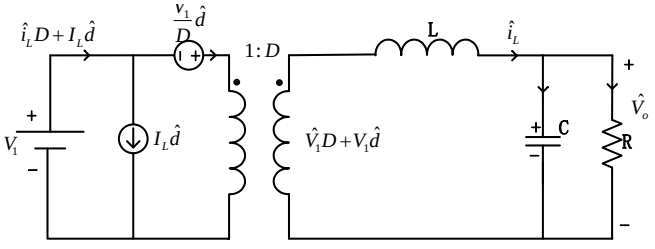

Fig. 4: The small-signal equivalent circuit model of buck converter

Table 1: Parameters of the small-signal equivalent circuit model.

Parameters	Values	Unit
Output inductor	10e-2	H
Resistance of load	20	Ω
Output storage capacitor	300e-6	F
Load	20	Ω
Switching frequency of the converter	2	*kHz*

The parameters of the small-signal model are given in Table 1, the transfer functions (13) and (14) can be easily obtained applying the Laplace transform in (12) assuming zero initial conditions

$$G_{vd}(s)=\frac{\hat{v}_o(s)}{\hat{d}(s)}=\frac{\frac{1}{cs}//R}{\frac{1}{cs}//R+Ls}=\frac{U_{in}}{s^2LC+sL/R+1} \tag{13}$$

$$\begin{aligned}G_{id}(s)&=\frac{\hat{i}_L(s)}{\hat{d}(s)}=\frac{\hat{v}_o(s)}{\hat{d}(s)}\frac{\hat{i}_L(s)}{\hat{v}_o(s)}=G_{vd}(s)\frac{\hat{i}_L(s)}{\hat{u}(s)}\\&=G_{vd}(s)\frac{1}{\frac{1}{Cs}//R}=\frac{1+sCR_0}{s^2LC+sL/R+1}\times\frac{U_{in}}{R_0}.\end{aligned} \tag{14}$$

Therefore, the open loop small-signal model without game theoretic control is obtained, and the bode plot of $G_{vd}(s)$ is shown as Fig. 5,

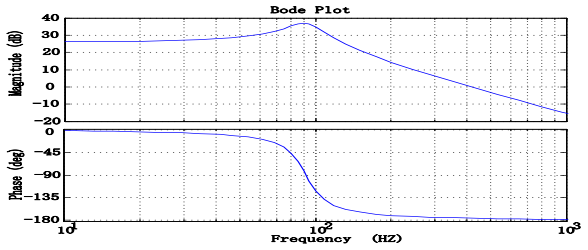

Fig. 5: The bode plot of $G_{vd}(s)$

As is shown in the Fig.5, phase margin is only about 10, the system is in a critical steady state. When the proposed game theoretic control is adopted, the close loop structure is illustrated in Fig.6.

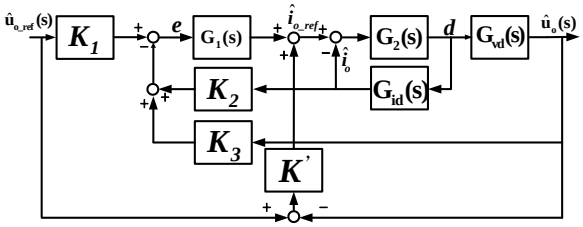

Fig. 6: The closed loop structure of circuit with game theoretic control

The equations of control are

$$\hat{i}_{o\_ref}=K\frac{1}{s}\times(k_1\hat{v}_{o\_ref}-k_2\hat{v}_o-k_3\hat{i}_o)+K'(\hat{v}_{o\_ref}-\hat{v}_o) \tag{15}$$

$$\hat{d}=(\hat{i}_{o\_ref}-\hat{i}_o)(K_P+K_I\frac{1}{s}). \tag{16}$$

Combine the (15) with (16)

$$\begin{aligned}\hat{d}&=K\frac{1}{s}\times(K_1\hat{v}_{o\_ref}-K_2\hat{v}_o-K_3\hat{i}_o)+K'(\hat{v}_{o\_ref}-\hat{v}_o)-\hat{i}_o]\times(K_P+K_I\frac{1}{s})\\&=[(KK_1\frac{1}{s}+K')\hat{v}_{o\_ref}-(KK_2\frac{1}{s}+K')\hat{v}_o-(KK_3\frac{1}{s}+1)\hat{i}_o]\times(K_P+K_I\frac{1}{s})\\&=[(KG_1(s)+K')\hat{v}_{o\_ref}-(KG_1(s)+K')\hat{v}_o-(KG_1(s)+1)\hat{i}_o]\times G_2(s)\end{aligned} \tag{17}$$

where $G_1(s)=K\frac{1}{s}$, $G_2(s)=K_P+K_I\frac{1}{s}$, $K=\frac{2BK_2}{A}$.

Assuming the input voltage $U_{in}=20V$, the parameters are given as fallows, $K=0.01$, $K'=0.5$, $K_P=0.5$, $K_I=1$, $K_1=1$, $K_2=0.8$, $K_3=0.2$. The open loop gain of current can be given by

$$T_{k\_i}(s)=G_2G_{id}=\frac{6\times10^{-2}s^2+10.12s^2+20}{6\times10^{-5}s^3+10^{-2}s^2+20s}. \tag{18}$$

Also, the bode plot can be obtained as Fig. 7.

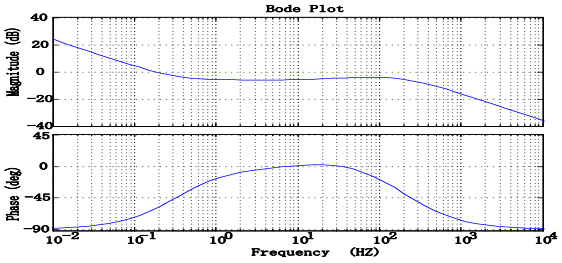

Fig. 7: The bode plot of current loop

As is shown in the Fig. 7, phase margin is about 110, the design of current loop is in a steady state. Therefore, the close loop structure with game theoretic control in Fig. 6 can be simplified as Fig. 8.

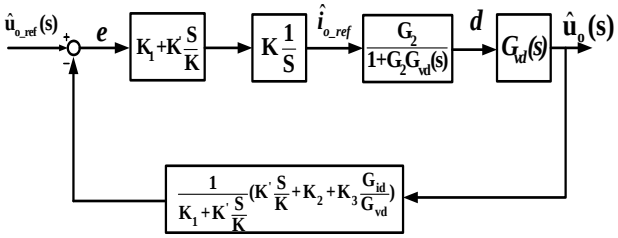

Fig. 8: The simplify close loop structure of circuit with game theoretic control

As is shown in the Fig. 8, the overall open-loop transfer function is obtained by

$$\begin{aligned}T_v(s)&=\frac{1}{K_1+K'\frac{S}{K}}(K'\frac{S}{K}+K_2+K_3\frac{G_{id}}{G_{vd}})\times(K_1+K'\frac{S}{K})\times K\frac{1}{S}\\&\times\frac{G_2}{1+G_2G_{vd}(s)}\times G_{id}(s)=\frac{G_2}{1+G_2G_{vd}}\times(KG_{id}+K_2K\frac{1}{S}G_{id}+KK_1\frac{1}{S}G_{id})\\&=\frac{3\times10^{-4}s^4+5.06\times10^{-2}s^3+100s^2+208s+0.2}{18\times10^{-11}s^6+24\times10^{-8}s^5+18.536\times10^{-5}s^4+8.5\times10^{-2}s^3+30.12s^2+20s}.\end{aligned} \tag{19}$$

Through the overall open-loop transfer function, the bode plot can be obtained as Fig. 9.

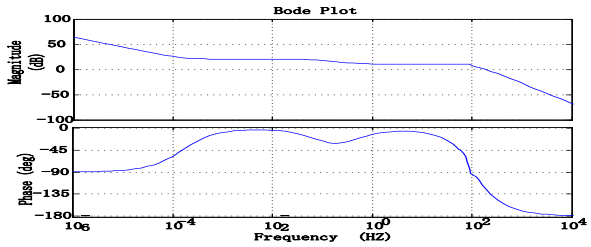

Fig. 9: The bode plot of overall open loop transfer function

From Fig. 9, it can be seen that phase margin is about 80, the system is in a steady state.

Through the small-signal model of the system control with game theoretic strategy, the design of the controller is stable.

IV. Numerical Simulation

In this part, by using the concept of virtual rival strategy, a system composed of two DGs with a resistive load and a storage device is used for simulate the micro-grid system. In this paper, we adopt the buck converter as the main circuit of controller. One DG is consisted of photovoltaic generator and its controller, and the other DG is consisted of wind turbine and its controller. The simulation structure of simplified system of micro-grid is shown as Fig.10, and the parameters of the model are as follows: the output inductor is 10e-2 H, the resistance of load is 20 Ω , the switching frequency adopt 2 kHz.

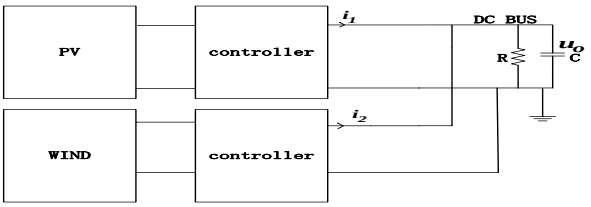

Fig. 10: Simulation structure of simplified system of micro-grid

A. Simulation Experiment

According to the design parameters above and the reference value of the DC line bus voltage is 20V. The results obtained from simulations in MATLAB are represented in Fig. 11, Fig. 12 and Fig. 13which show the state of micro-grid with different control methods. The current of each DG is shown in the upper picture, and voltage of DC line bus is shown in the lower picture. At the upper picture, the two curves indicate the current of photovoltaic generator and wind generator circuit respectively.

When two DGs are adopted open loop control, the results of current share mainly depend on the symmetry of module parameters. As is shown in the Fig. 11, it is clear that the voltage is maintained in 20V and the performance of the current sharing is bad. Although using the open loop control can meet the voltage regulation, the performance of the current sharing is not ideal.

When the micro-grid system adopt the droop control strategy, as is shown in Fig. 12, it is clear that the output current of each circuit is almost the same, and the error of current is less than 5%. However, the voltage of DC bus is only maintained about 17V which causes a drop in voltage regulation. Although using the traditional droop strategy can meet the request of output current sharing, the regulation of DC line bus voltage is not ideal.

Compared with the traditional droop control strategy and directly parallel strategy, the game controller has a good performance on voltage regulation and current sharing. As is shown in the Fig. 13, it is clear that the output current of each circuit is almost the same and the voltage is maintained in 20V. In addition, the regulation time of game system is as long as the traditional controllers which adopt the droop strategy. In conclusion, the game theoretic method is possible to control each system rapidly and independently.

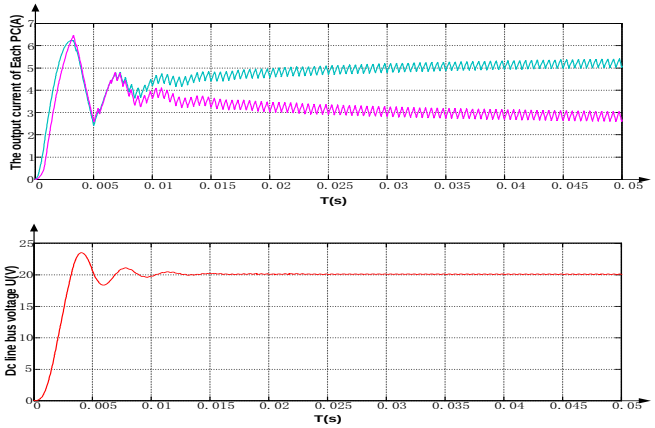

Fig.11: State of micro-grid system with the open loop control strategy

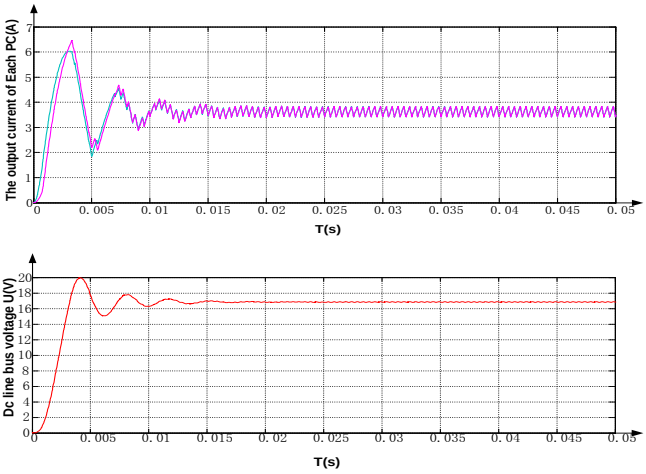

Fig.12: State of micro-grid system by droop control method

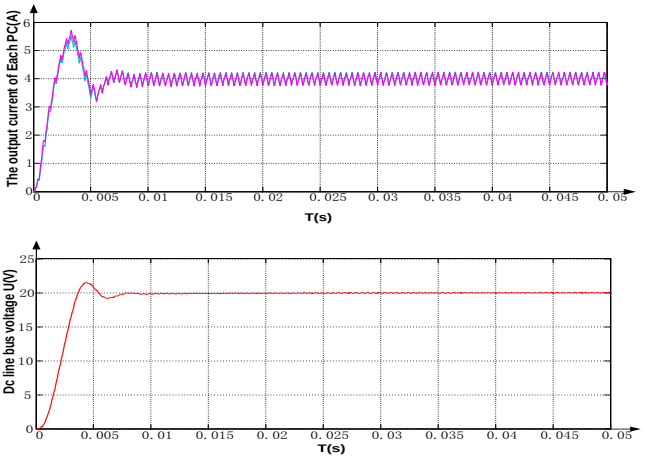

Fig.13: State of micro-grid system by game theoretic strategy method

B. Dynamic Response

In order to study the controller performance to large transients, a variable load is implemented (a load of 10Ω is turned on in the micro-grid output). In this part, the reference value of the DC line bus voltage is 24V. The Fig. 14, Fig. 15 and Fig. 16 show the load change in the micro-grid when time arrive at 0.05s.

Fig. 14, Fig. 15 and Fig. 16 present the experiments for a load step from 100% to 50% of the output power. During this transient, an overshoot of less than 5% is observed in the output voltage with a good regulation as required. At the same time, the current of each DG changes synchronously, which achieves current sharing state finally.

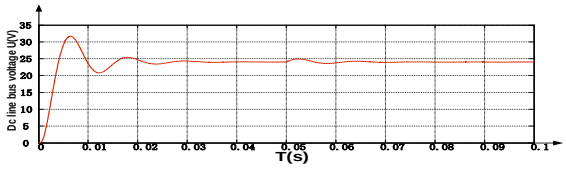

Fig.14: Voltage of dc line bus when load change in 0.05s

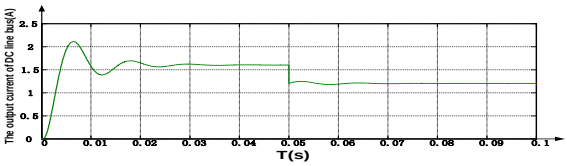

Fig.15: Current of dc line bus when load change in 0.05s

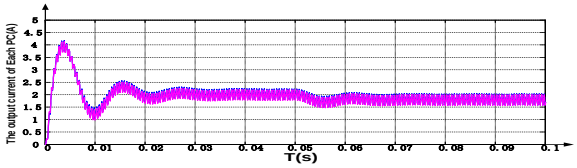

Fig.16: Current of each PC when load change in 0.05s

C. Experimental Result

An experimental result is produced by laboratory prototype, as shown in Fig. 17. This prototype consists of two PV simulators, and their buck converters connected to a stand-alone DC system which has an output storage ultra-capacitor and an adjustable resistive load. The simplified system is shown in Fig. 10.

The Fig. 17 and Fig. 18 show the measured waveform for a step load increase. 100% load is increased at t = 370s, causing a transient step up of the output current waveforms of two DGs. The experimental results of the microgrid voltage are depicted in Fig. 17, which shows the change of the DC bus voltage due to the variations of the load. Fig. 18 shows the output current of each DG converter. During the dynamic process, the current sharing is achieved by the two DGs. The measured current waveforms in Fig. 17 show the rapid response of the current-regulated. At the same time, the voltage of DC bus keeps the reference value stable in 24V.

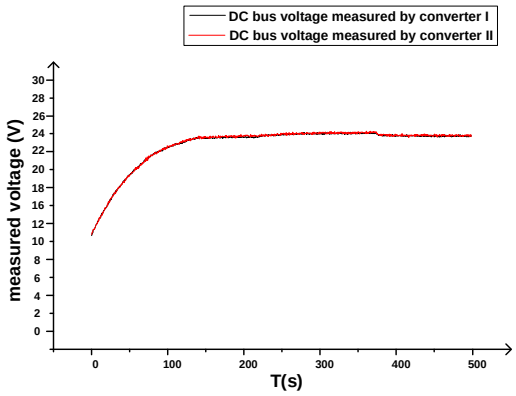

Fig. 17: Measured voltage of each converter when load steps increase at 370s

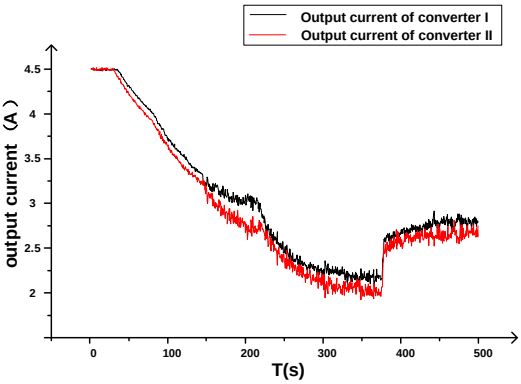

Fig. 18: Measured output current of each converter when load steps increase at 370s

V. Conclusion

In this paper, the game controller is applied to DGs and it can be seen that using this method achieves desired performance in voltage regulation and current sharing among the micro-grid system. In order to simplify the analysis, we adopt the concept of virtual rival strategy that simplifies the n-player-game problem to two-player-game problems.

A small-signal stability analysis of the proposed control approach was shown. In addition, the proposed approach has been tested extensively in simulation. The controller allows DGs to share power generation without communications, and the performance of dynamic response is obtained by experimental results. It is concluded that the new control strategy shows good results in transient issues, power sharing, and stability.

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BIOGRAPHIES

Mingxuan Wu obtained his Bachelor degree and master degree from Beijing Institute of Technology. He is currently an engineer in the Department of China Southern Power Grid. His research interests are in the areas of DC microgrid system and new energy power generation.

Lei Dong was born in 1967. He is currently a professor in Beijing Institute of Technology.His research directions are power electronics and power drive,and new energy power generation.

Furong Xiao obtained his bachelor degree from the Beijing Institute of Technology in 2011,and still study for the PHD degree in this school. His research direction is power energy conversion and micro grid.

Xiaozhong Liao was born in Guangdong, China, in 1962. She received her BSc and PhD degrees respectively from the Tianjin University in electrical and automation engineering and the Beijing Institute of Technology in control engineeering. She is currently a professer in Beijing Institute of Technology. Her research intersts are the electric drive system and energy converter control.

Three Phase Double Boost PFC Rectifier Fed SRM Drive

M. Rajesh [1] B. Singh [2]

Abstract: **This paper deals with a three phase double boost PFC(power factor correction) rectifier fed SRM (Switched Reluctance Motor) drive. The proposed system consists of two boost converters with DC outputs connected in series to feed a midpoint converter fed SRM drive. This system needs only two active switches at rectifier side and a midpoint converter needs only one active switch per phase. Besides, it provides balanced DC link capacitor voltages with improved power quality at AC mains. The proposed three phase double boost PFC rectifier fed SRM drive is designed, modeled and its performance is simulated in MATLAB/Simulink. The performance of proposed system is compared with a six pulse diode bridge converter fed SRM drive.**

Keywords–Midpoint converter, power quality, switched reluctance motor, Boost PFC rectifier, Scott transformer.

I. INTRODUCTION

A switched reluctance motor (SRM) has the simplest construction and is economical among other electrical motors. It has several advantages as a variable speed drive as it can operate in wide speed range. However SRM cannot be operated directly from AC or DC supply, it requires power converts for its operation. The most commonly used converter is a midpoint converter since only one switch per phase is needed thus reducing the cost of drive [1]. All these converters need DC supply or AC supply with a rectifier. Fig.1 shows six pulses diode bridge rectifier fed midpoint converter based SRM drive. The disadvantage of this configuration is that it generates harmonics to the AC mains with low input power factor.

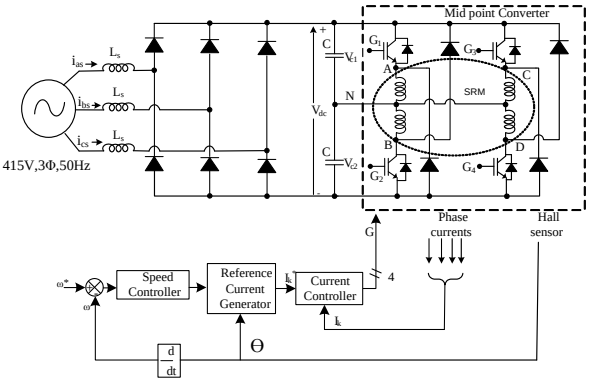

Fig.1: Six pulse diode bridge rectifier fed SRM drive

Three phase active PFC boost rectifiers are preferred in industries due to their high efficiency, low EMI emission and improved power quality at AC mains. Most commonly used PFC boost rectifiers are multilevel boost rectifier, Vienna rectifier and third harmonic modulated rectifiers. Different configurations of multilevel rectifiers are given in [2-5]. Multilevel reduce the voltage stress across active switches and operate at lower frequencies. However, these rectifiers need more number of active switches and control of capacitor voltages becomes difficult with increase in levels. A simple three phase NPC three level rectifier needs twelve active switches. The multilevel rectifiers are capable of operating in all four quadrants [6]. Vienna rectifier [7-12] is a boost rectifier which requires only three active switches and its control is simple. This rectifier has short circuit immunity to failure of control circuit, immunity towards voltage unbalance and voltage variations. Third harmonic modulated rectifier is explained in [13-15]. It consists of third harmonic current injection network to inject third harmonic current at AC side of rectifier to improve power quality at AC mains.

Minnesota rectifier [16] is one of the most commonly used rectifier which uses third harmonic current injection technique. This rectifier needs only two active switches and a zig zag transformer is used to inject third harmonic current at AC side of rectifier. All these converter topologies do not provide isolation. However in many applications isolation is required between AC mains and the drive.

Three phase double boost PFC rectifier fed midpoint converter based SRM drive is recommended in this paper for improving power quality at AC mains. In this system the outputs of two single phase boost PFC rectifier are connected in series to form split DC bus voltage. The input of these boost rectifiers is connected to Scott connected transformer which provides isolation. The voltage stress on the active switches and the diodes of this boost rectifier is equal to half of DC link voltage. The proposed SRM drive is designed, modeled and its performance is simulated using MATLAB/Simulink environment and the performance is also compared with a conventional six pulse diode bridge rectifier fed SRM drive. The power quality of the proposed drive system is found within IEEE 519 standard limit [17].

II. SYSTEM CONFIGURATION

The schematic diagram of three phase double boost PFC rectifier fed midpoint based SRM drive is shown in Fig.2a. Two single phase AC supplies with 90^0 phase shift are obtained from Scott connected transformer and given to two single phase boost rectifier. The outputs of single phase boost rectifiers are connected in series and form split DC bus voltages which are connected to a midpoint converter based SRM drive. The connection diagram and phasor diagram of Scott connected transformer is shown in Fig.2b. Two single phase transformers are used to obtain three phase to two single phase conversion. One of the transformers is called teaser transformer and has the turns ratios of $0.866V:V_1$ and other transformer called main transformer has midpoint at primary winding having turns ratio of $0.5V - 0.5V:V_2$. Where V is the magnitude of

The paper first received 23 Jan 2013 and in revised form 14 July 2013.
Digital Ref: APEJ-2013-05-419

[1] Department of Electrical Engineering, Indian Institute of Technology Delhi, E-mail: mrajeshkerala@gmail.com
[2] Department of Electrical Engineering, Indian Institute of Technology Delhi E-mail: bsingh@ee.iitd.ac.in

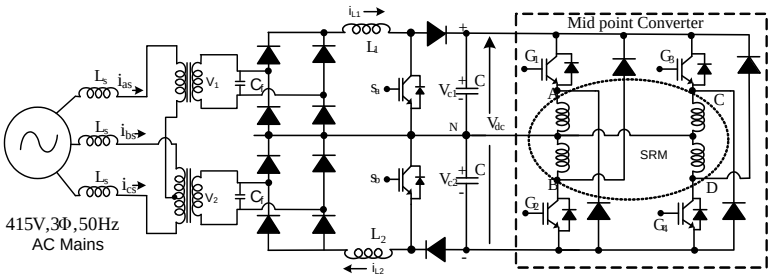

Fig.2 (a): Three phase double boost PFC rectifier fed SRM drive diagram

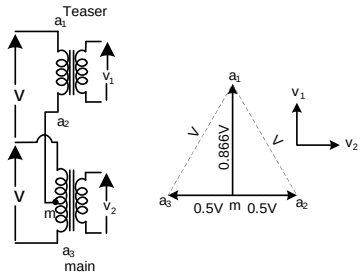

Fig.2 (b): Scott connected transformer and its phasor

supply line voltage, V_1 and V_2 are secondary voltages of

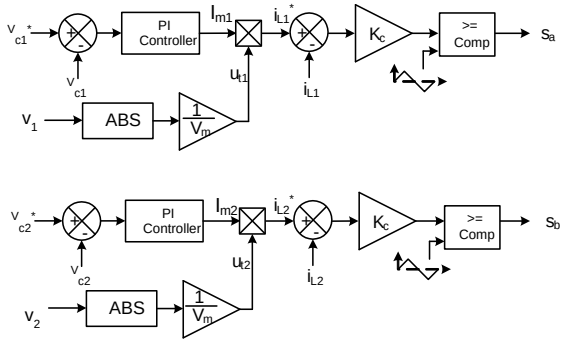

Fig.2 (c): Control of three phase double boost PFC rectifier

the transformers. Two single phase boost rectifiers are controlled independently by sensing their inductor currents. A small rating capacitor C_f is connected at the secondary terminals to eliminate higher order harmonics.

III. Design of Three Phase Double Boost PFC Rectifier

Three phase double boost PFC rectifier consists of a two single phase transformers, two boost inductors, two DC link capacitors, two active switches and ten diodes. The design of proposed converter system is explained below.

A. Design of Boost Inductor

For a 4kW, 8/6 pole SRM drive, an input power is considered as 4.4kW including losses. The value of boost inductor ($L=L_1=L_2$) is calculated as [18],

$$L = \frac{V_{in} D}{\Delta I f_s} \tag{1}$$

where V_{in} and D are defined as,

$$V_{in} = \frac{2\sqrt{2}V_1}{\pi} \tag{2}$$

$$D = \frac{V_{c1} - V_{in}}{V_{c1}} \tag{3}$$

where V_{in} is the DC output voltage of bridge rectifier, V_1 is the secondary terminal voltage of transformer, D is duty ratio, ΔI is the inductor ripple current, V_{c1} is the output voltage of boost rectifier and f_s is switching frequency.

The input power 4.4kW is shared by PFC boost rectifier equally. Hence the supply current drawn by the boost rectifier with transformer secondary voltages $V_1 = V_2 = 180V$ is calculated as,

$$I = \frac{P_{boost}}{V_1} = \frac{2200}{180} = 12.22A \tag{4}$$

Since same current flows through inductor the ripple current (ΔI) in the inductor at 12% ripple is calculated as,

$$\Delta I = 10\% \text{ x } I = 1.222A \tag{5}$$

Taking duty switching frequency f_s as 20 kHz, DC link voltage V_{dc} as 560V and V_{c1} as 280V ($V_{dc}/2 = 560/2$), from eqns. (1-5), the obtained value of boost inductor is L is 2.8mH, hence L_1 and L_2 are selected as $L_1 = L_2 = 3mH$.

B. Design of Capacitor

To assure DC link voltage within limit for three phase double boost PFC rectifier the DC link capacitor (C_1, C_2) is calculated as [18],

$$C_1 = C_2 = \frac{I_d}{2\omega \Delta V_{c1}} \tag{6}$$

where ΔV_{c1} is the ripple voltage across capacitor, $\omega = 2nf$ is angular frequency of supply voltage and f is supply frequency and I_d is DC link current.

DC link current I_d is calculated as,

$$I_d = \frac{P_{in}}{V_{dc}} \tag{7}$$

Taking P_{in} as 4.4kW, V_{dc} as 560V, f as 50Hz and ΔV_{c1} as 2% of V_{c1}, the obtained value of I_d is 7.851A and obtained value of C_1 is 2233µF, hence C_1 and C_2 are selected as 2200µF.

C. Design of Transformer

For converting three phase 415V AC mains to two single phase voltages of each of 180V, the required turns ratio(n_1, n_2) of single phase transformers needed for Scott's connection is calculated as,

$$\text{Teaser transformer } n_1 = \frac{0.866V}{V_1} \tag{8}$$

Main transformer $n_2 = \dfrac{0.5V - 0.5V}{V_2}$ (9)

where V is the AC mains voltage, V_1 and V_2 are secondary voltage of transformers, with V = 415V and $V_1 = V_2$ as 180V, the calculated value of turns ratio are n_1 = 359.5/180 and n_2 = 207.5-207.5/180.

IV. Control of Three Phase Double Boost PFC Rectifier FED SRM Drive

The control algorithm of three phase double boost PFC rectifier is shown in Fig.2c. The boost rectifiers are controlled independently by sensing boost inductor current. The gate signals are generated by carrier based PWM controller. Each boost rectifier consists of capacitor voltage controller, reference boost inductor current estimator and boost inductor current controller.

A. Capacitor Voltage Controller

The reference capacitors voltages (V_{c1}^* and V_{c2}^*) of two boost PFC rectifier are compared with the sensed capacitors voltages (V_{c1} and V_{c2}). The resulting capacitors voltage errors (V_{c1e} and V_{c2e}) at nth instant are given as,

$$V_{c1e}(n) = V_{c1}^*(n) - V_{c1}(n) \quad (10)$$

$$V_{c2e}(n) = V_{c2}^*(n) - V_{c2}(n) \quad (11)$$

The PI (Proportional Integral) voltage controllers are used to get reference currents I_{m1}^* and I_{m2}^* and are given at nth sampling instant as,

$$I_{m1}^*(n) = I_{m1}^*(n-1) + K_{p1}\{V_{c1e}(n) - V_{c1e}(n-1)\} + K_{i1}V_{c1e}(n) \quad (12)$$

$$I_{m2}^*(n) = I_{m2}^*(n-1) + K_{p1}\{V_{c2e}(n) - V_{c2e}(n-1)\} + K_{i1}V_{c2e}(n) \quad (13)$$

where the outputs of capacitor voltage controllers at nth are $I_{m1}^*(n)$ and $I_{m2}^*(n)$ and for (n-1)th instant are $I_{m2}^*(n\text{-}1)$ and $I_{m2}^*(n\text{-}1)$. These capacitors voltage error at nth instant is given by $V_{c1e}(n)$ and $V_{\backslash c2e}(n)$ and for (n-1)th sampling instant are $V_{c1e}(n\text{-}1)$ and $V_{\backslash c2e}(n\text{-}1)$; K_{p1} and K_{i1} are proportional and integral gains of the DC capacitor voltage controllers.

B. Reference Boost Inductor Current Estimation

Unit templates of secondary side voltage of Scott's transformer are given as,

$$u_{t1}(\omega t) = \frac{abs(v_1(\omega t))}{V_m} = |\sin(\omega t)|; \quad u_{t2}(\omega t) = \frac{abs(v_2(\omega t))}{V_m} = |\sin(\omega t - 90^0)| \quad (14)$$

where V_m is the amplitude of transformer secondary voltages.

The reference inductors currents (i_{L1}^* & i_{L2}^*) are estimated as,

$$i_{L1}^* = I_{m1}^* u_{t1}(\omega t) \text{ and } i_{L2}^* = I_{m2}^* u_{t2}(\omega t) \quad (15)$$

C. Boost Inductor Current Controller

Fig.2c shows the controller of the three phase double boost PFC rectifier. The reference boost inductor currents are compared with sensed currents and the current error is processed through a proportional current controller of gain K_c. This output of current controller is fed to the carrier based PWM generator. The carrier based PWM generator consists of a comparator and a triangular carrier wave of 20kHz. The output of current controller is compared with carrier wave to generate PWM signal and given to switches S_a and S_b.

V. Control of SRM

The rotor speed of SRM is compared with reference speed and the speed error is processed through a speed proportional integral (PI) controller. The error speed ($\Delta\omega_e$) at nth instant is given as,

$$\Delta\omega_e(n) = \omega_e^*(n) - \omega_e(n) \quad (16)$$

The PI speed controller generates reference motor current magnitude I* and at nth sampling instant the magnitude of reference current is given as,

$$I^*(n) = I^*(n-1) + K_{p2}\{\omega_e(n) - \omega_e(n-1)\} + K_{i2}\omega_e(n) \quad (17)$$

where $I^*(n)$ and $I^*(n\text{-}1)$ are magnitude of reference phase current of SRM at nth and (n-1)th sampling instants. K_{p2} and K_{i2} are proportional and integral gain constants of the PI speed controller. This reference current magnitude is given to reference current generator. The reference current generator generates all four phases reference currents by multiplying unit pulse obtained from Hall effect position sensors.

Reference current of kth phase of SRM is given as,

$$I_k^* = I^* U_k \quad (18)$$

where U_k is unit pulse of k^{th} phase obtained from the information of Hall effect position sensor, turn on and turn off angles.

The phase currents SRM windings are compared with generated reference currents and given to the hysteresis current controller. The output of hysteresis current controller is used for gating insulated gate bipolar transistors IGBT (G_1) - IGBT (G_4) of a midpoint converter.

The angle where the IGBT of the phase of SRM is excited is called turn on angle (Θ_{on}) and the angle at which IGBT of the phase of SRM winding is turned off is called turn off angle (Θ_{off}). If the phase commutation is made faster by adjusting Θ_{on} and Θ_{off}, the current in the winding increases at minimum inductance position and thereby getting the advantage of reducing the current before the rotor reaches the negative torque region. This is achieved by advancing Θ_{on} by an advance angle (Θ_{adv}) from the position Θ_m where the inductance starts increasing. The

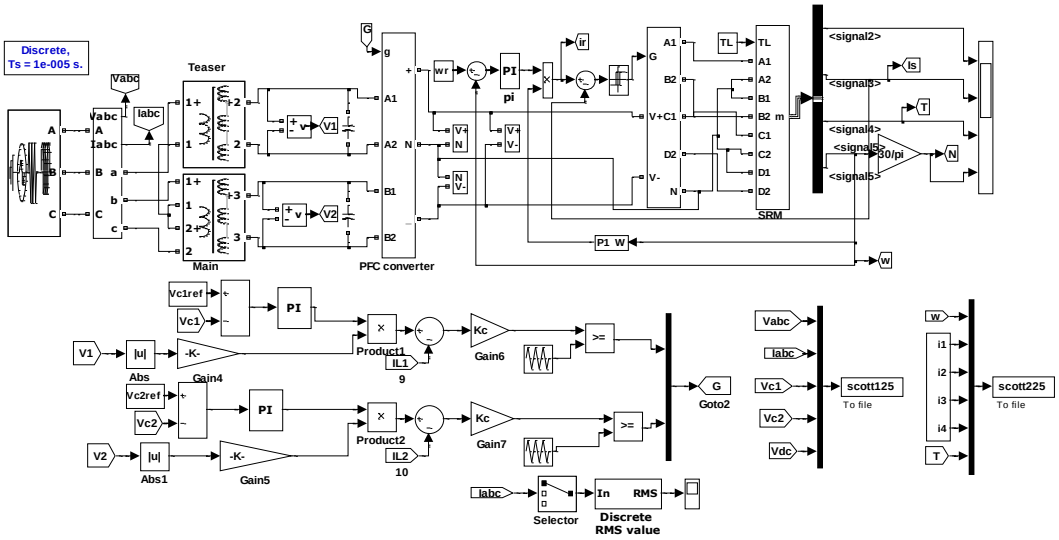

Fig.3. Matlab model of three phase double boost PFC rectifier fed SRM drive.

advance angle (Θ_{adv}) is calculated as per following equation.

Near turn on the voltage - Ampere equation can be approximated as,

$$V_{c1} = \frac{\partial \varphi}{\partial i}\frac{di}{dt} = L_u \frac{di}{dt} \tag{19}$$

Using first order approximations, (19) can be written as,

$$V_{c1} = L_u \frac{di}{d\theta}\frac{d\theta}{dt} = L_u \frac{di}{d\theta}\omega \tag{20}$$

(18) is used for calculating advance angle, Θ_{adv} as,

$$\theta_{adv} = \frac{L_u i_p}{V_{C1}}\omega \tag{21}$$

where L_U is the unaligned inductance, V_{c1} ($=V_{dc}/2$) is the applied voltage across a phase of SRM, ω angular speed and i_p is the desired phase current of SRM for obtaining required torque.

Turn on angle (Θ_{on}) to achieve desired phase current i_p at Θ_m is given as,

$$\theta_{on} = \theta_m - \theta_{adv} \tag{22}$$

VI. MATLAB BASED MODELING OF PROPOSED SRM DRIVE

The developed MATLAB/Simulink model of three phase double boost PFC rectifier fed midpoint convert based SRM drive is shown in Fig.3. A filter capacitor is used at line to reduce higher order harmonics. Three phase 415 V, 50 Hz AC supply voltage is fed to a three phase double boost PFC rectifier based SRM drive. The reference DC link capacitor voltages (V_{c1}, V_{c2}) are selected as 280V and the reference speed (ω_r) is considered as 157.08rad/sec. The rating of SRM and other data are given in Appendix. The data of SRM motor used in this simulation is obtained from experimental data of 4kW, 8/6 pole, 1500rpm. Turn on angle is selected as per (21-22).

VII. RESULTS AND DISCUSSION

The performance of proposed three phase double boost PFC rectifier fed midpoint convert based SRM drive is simulated and the performance is compared with a conventional six pulse diode bridge converter fed SRM drive. The simulated results are shown in Fig.4a-5e , V_{sph} and I_s represent AC mains phase voltage and line currents. I_a represents line current of AC mains phase A. $I_1 - I_4$ represents the phase currents of SRM. ω is motor speed in rad/sec and T is the developed motor torque in Nm. Simulated results of six pulse bridge rectifier fed SRM drive at 25Nm load torque are shown in Fig.4a-4b. The simulated results show that at rated load torque, the supply current THD is 61.7%, CF (crest factor) is 2.1754 and the supply rms current(I_{rms}) is 6.9A. Hence the supply current THD and CF of six pulse rectifier fed SRM drive are very high which are not within the limits of IEEE -519 standard [17].

Simulated results of the proposed three phase double boost PFC rectifier fed SRM drive at rated load torque of 25Nm are shown in Figs.5a-5b. The steady state response at rated load is shown in Fig.5a and its harmonic spectrum of supply current is shown in Fig.5b. Simulated results of the proposed drive system show that at rated load the supply current THD is 2.04%, CF(crest factor) is 1.4224 and the supply rms current(I_{rms}) is 6.05A. Simulated results of the proposed SRM drive at 20% rated load torque of 5Nm are shown in Figs.5c-5d. Simulated results show that at 20% of rated load torque the supply current THD is 4.23%, CF(crest factor) is 1.3928 and the supply rms current(I_{rms}) is 2.15A. Hence these results show that the THD and CF of AC mains current for the proposed drive are within IEEE - 519 standard limit [17]. Fig.5e shows the dynamic response of proposed drive. Steady state operation is reached in 0.255s and the starting current is well within the limit.

Table 1 shows the performance of six pulse diode bridge converter fed SRM drive at different loads. It is seen that the THD and CF of AC mains current of six pulse diode bridge converter fed SRM shown are very high and power factor is very low even at full load. Table 2 shows the performance of proposed three phase double boost PFC

rectifier fed SRM drive at different loads. It is observed that the THD and CF of AC mains current of proposed drive are well within the limit for all loads and the power factor is also very high even at light loads.

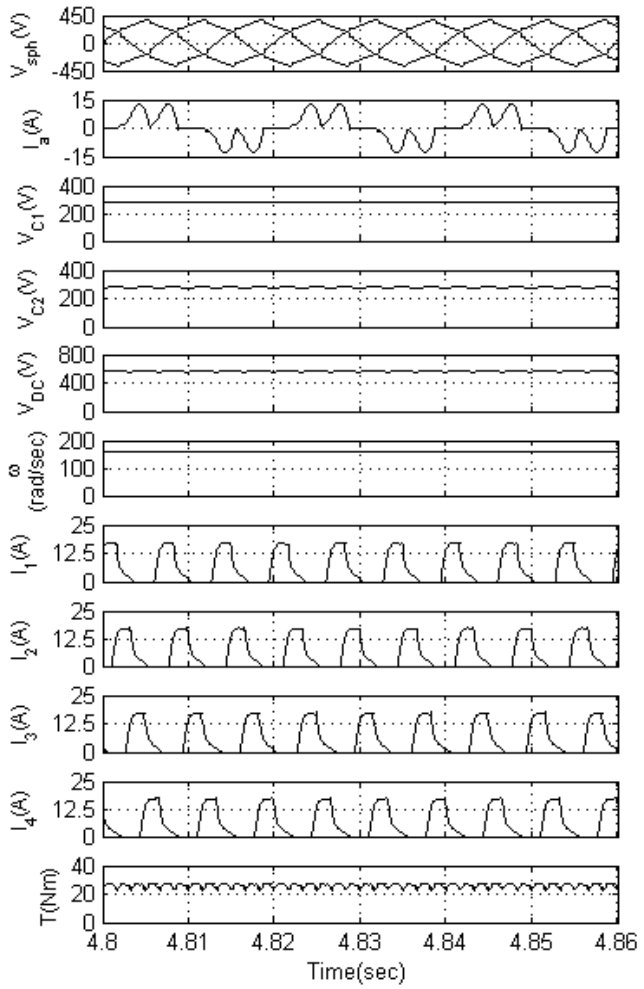

Fig.4 (a): Steady state response of six pulse AC-DC converter fed SRM drive at rated torque of 25Nm.

VIII. CONCLUSION

The proposed three phase double boost PFC rectifier fed midpoint converter based SRM drive has been designed and modeled using MATLAB/Simulink environment. The performance of proposed SRM drive has been compared with a six pulse converter fed SRM drive. A three phase double boost PFC rectifier fed SRM drive along with capacitor filter on secondary winding of the transformer has reduced the THD of supply current to less than 5%. The THD and CF of AC supply current have been maintained within IEEE - 519 standard limit even with 20% rated load torque with a high power factor. The dynamic response of the proposed three phase double boost PFC rectifier fed SRM drive has shown the smooth operation which is required in many industrial applications. The ripple in DC link voltage is found negligible and the voltages across the capacitors are found well balanced which is needed for smooth operation of SRM.

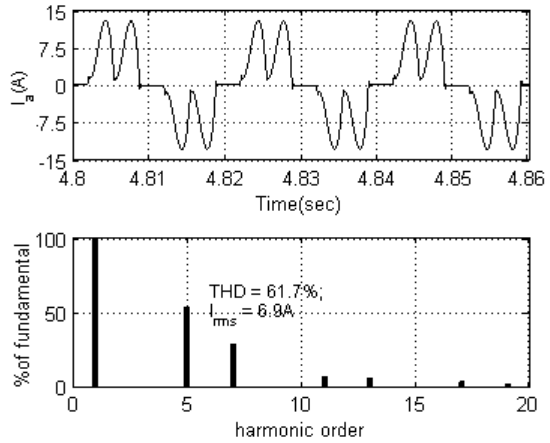

Fig.4 (b): Harmonic spectrum of six pulse AC-DC converter fed SRM drive at rated torque of 25Nm.

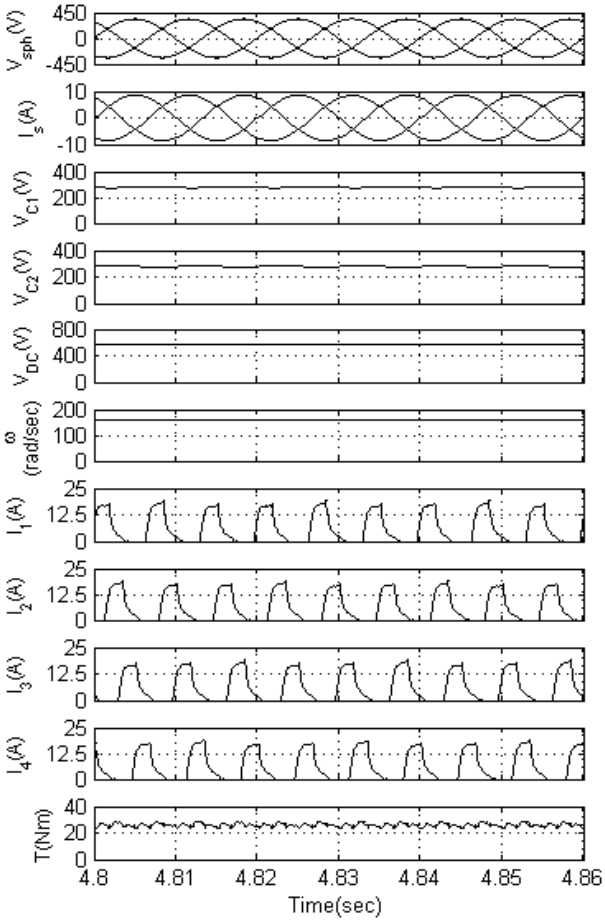

Fig.5 (a): Steady state response of three phase double boost PFC rectifier fed SRM motor drive at rated torque of 25Nm.

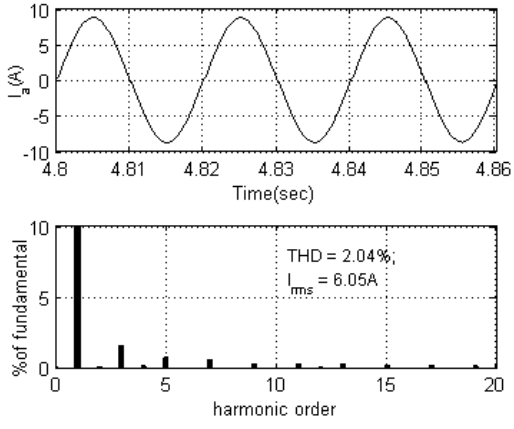

Fig.5 (b): Harmonic spectrum of three phase double boost PFC

rectifier fed SRM motor drive at rated torque of 25Nm.

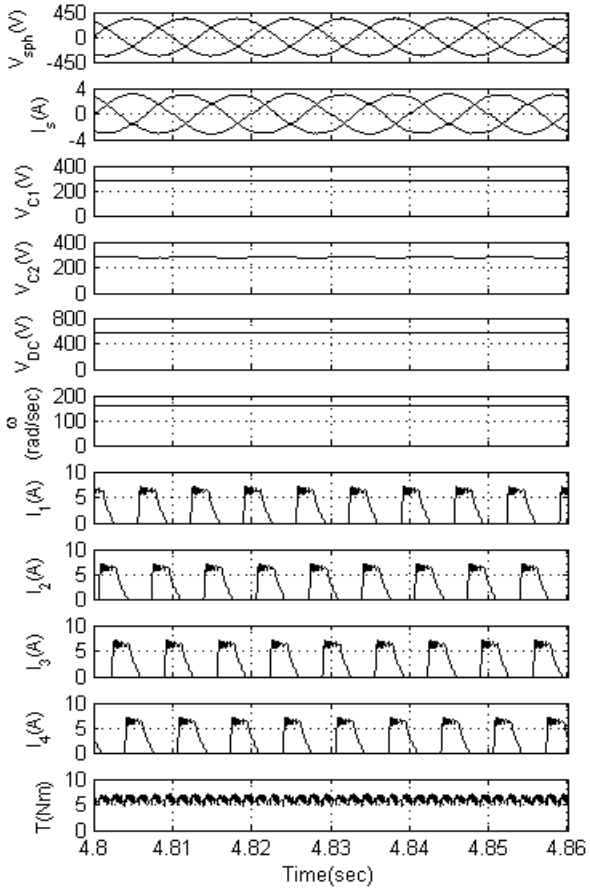

Fig.5 (c): Steady state response of three phase double boost PFC rectifier fed SRM motor drive at 20% rated torque of 5Nm.

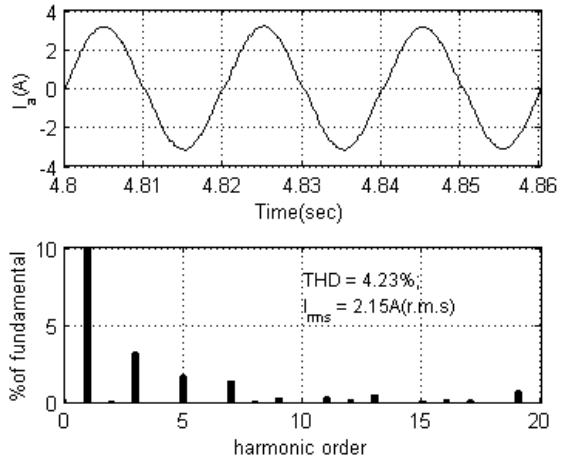

Fig.5 (d): Harmonic spectrum of three phase double boost PFC rectifier fed SRM motor drive at 20% rated torque of 5Nm

Table 1: Performance of six pulse AC-DC converter FED SRM drive at varying load torque at 415V supply voltage

T_L(N.m)	THD %	I_{rms} (A)	CF	DPF	DF	PF
5	91.43	2.81	2.8675	1	0.405	0.405
10	83.47	3.85	2.6378	1	0.551	0.5507
15	77.18	4.90	2.4852	1	0.636	0.6359
20	70.07	5.93	2.3270	1	0.713	0.7135
25	61.70	6.90	2.1754	1	0.787	0.787

Table 2: Performance of three phase double boost PFC rectifier FED SRM motor drive at varying load torque at 415V supply voltage

T_L(N.m)	THD %	I_{rms} (A)	CF	DPF	DF	PF
5	4.23	2.15	1.39276	1	0.999	0.999
10	3.20	3.00	1.35878	1	0.999	0.999
15	2.65	4.00	1.41343	1	1.000	1.000
20	2.30	5.00	1.40562	1	1.000	1.000
25	2.04	6.05	1.42243	1	1.000	1.000

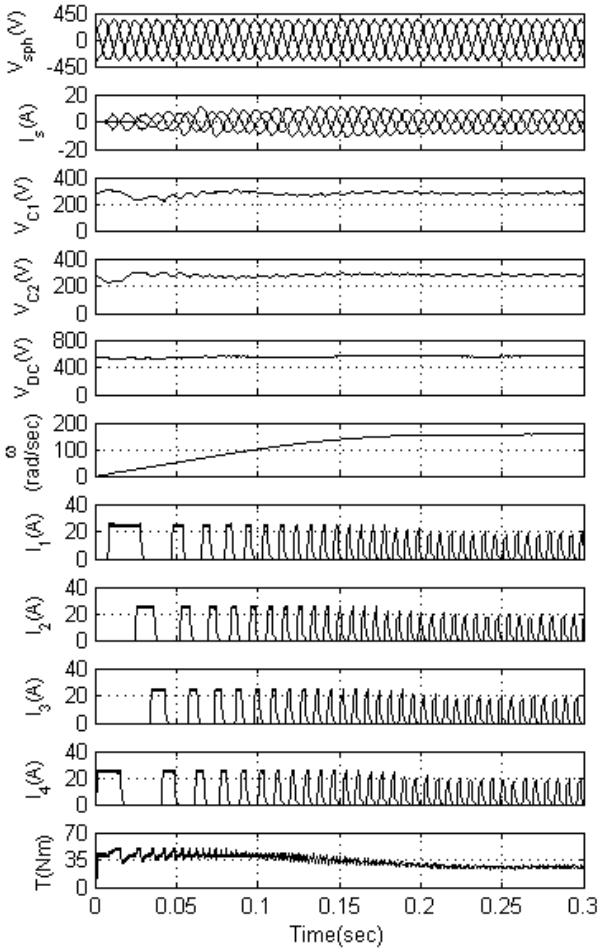

Fig.5 (e): Dynamic response of three phase double boost PFC rectifier fed SRM motor drive at rated torque of 25Nm.

APPENDIX

Switched Reluctance Motor Specifications:
4kW, 8/6pole, 1500rpm, R (Phase Resistance) =0.7 Ω, L_u (unaligned inductance) = 12mH, L_a (aligned inductance) = 110mH, J=0.016kg-m^2, B=0.0065Nms.
Reactor: Boost inductor L = 3mH
Midpoint Converter Capacitors: $C_1 = C_2$ = 2200 μF.
AC Mains: 415 V $_{L\text{-}L}$, 50 Hz, source inductance, L_s = 2mH, R_s = 0.09Ω.
Passive Filter Parameters: C_f = 5 μF.
Transformer:
Teaser transformer- 2.5kVA, 359.4V/180V
Main transformer- 2.5kVA, 207.5V-207.5V/180V
Gains of PI Controllers: K_c=40, K_{p1} = 0.01, K_{i1} = 20, K_{p2} = 0.077, K_{i2} = 50.

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BIOGRAPHIES

M. Rajesh received his B.Tech. in Electrical and Electronics Engineering from the University of Calicut, Kerala, in 1995 and his M.Tech. in Power Electronics and Drives from the National Institute of Technology Warangal(NITW), Warangal, Andhra Pradesh, in 2005. In 2000, he joined Department of Electrical Engineering and Electronics Engineering, Govt: College of Engineering, Kannur, Kerala as a Lecturer. He is currently on deputation for doing research at Department of Electrical Engineering, IIT Delhi. His area of interest includes power quality improvements, power electronics and drives.

Bhim Singh received the Bachelor of Engineering (Electrical) degree from the University of Roorkee, Roorkee, India, in 1977, and M.Tech. (Power Apparatus and Systems) and Ph.D. degrees from the Indian Institute of Technology Delhi (IITD), New Delhi, India, in 1979 and 1983, respectively. In 1983, he joined the Department of Electrical Engineering, University of Roorkee, as a Lecturer. He became a Reader there in 1988. In December 1990, he joined the Department of Electrical Engineering, IIT Delhi, India, as an Assistant Professor. Where he has became an Associate Professor in 1994 and a Professor in 1997.

He has received Khosla Research Prize of University of Roorkee in the year 1991. He is recipient of JC Bose and Bimal K Bose awards of The Institution of Electronics and Telecommunication Engineers (IETE) for his contribution in the field of Power Electronics. He is also a recipient of Maharashtra State National Award of Indian Society for Technical Education (ISTE) in recognition of his outstanding research work in the area of Power Quality. He has received PES Delhi Chapter Outstanding Engineer Award for the year 2006.

He has been the General Chair of the IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES'2006) held in New Delhi. He has guided 42 Ph.D. dissertations 139 ME/M.Tech theses and 60 BE/B.Tech. projects. He has been granted one US patent and filed ten Indian patents. He has executed more than sixty sponsored and consultancy projects.

His fields of interest include power electronics, electrical machines, electric drives, power quality, FACTS (flexible ac transmission systems), HVDC (High voltage direct current) transmission systems.

Prof. Singh is a Fellow of the Indian National Academy of Engineering (FNAE), The National Academy of Science, India (FNASc), The Indian Academy of Sciences, India (FASc), Institute of Electrical and Electronics Engineers (FIEEE), the Institute of Engineering and Technology (FIET), Institution of Engineers (India) (FIE), and Institution of Electronics and Telecommunication Engineers (FIETE) and a Life Member of the Indian Society for Technical Education (ISTE), System Society of India (SSI), and National Institution of Quality and Reliability (NIQR).

A Novel Seven-Level Inverter System for DTC Induction Motor Drive

O.C. Sekhar [1] K.C. Sekhar [2]

Abstract–This paper presents the novel multilevel inverter fed control structure for induction motor based Direct Torque Control (DTC) strategy using a seven-level Multi Point Clamped (MPC) Voltage Source Inverter (VSI) is presented. It is shown that the multilevel topology presents enough degrees of freedom to control both electromagnetic torque and stator flux with very low ripple and high dynamics on other side. Simulation results, obtained with conventional or two-level, three-level inverter, five-level and seven-level inverter fed DTC induction motor (IM) drive, are presented and compared. This analysis shows that feeding electrical drive with multi level inverter can greatly improves the drive performance. The performance of this control method has been demonstrated by simulations performed using a versatile simulation package, MATLAB/SIMULINK.

Keywords–DTC, seven-level MPC VSI, induction motor, MATLAB/SIMLINK.

I. INTRODUCTION

Electrical vehicle applications require frequent torque control to adjust the speed of a vehicle. This has resulted in the need for a control scheme with high performance, fast transient, and accurate control of torque for an induction motor drive. The two most popular schemes for this are the vector control and the direct torque control (DTC) [1], [2]. The DTC schemes proposed by [3], and [4] (as a direct self-control) have several variations to the original structure, such as to overcome the inherent disadvantages in any hysteresis-based controller with variable switching frequency, high sampling requirement for digital implementation, and high torque ripple [5]–[11] Recently, predictive control strategy [12]–[14], dithering technique [15], sliding mode control [16], fuzzy logic control [17], and support vector machine (SVM) [10], [18]–[20] have found applications in motor drives. Furthermore, the use of these control schemes during a large step change in torque command does not guarantee the fastest torque response.

Multilevel power conversion technology is a very rapid growing area of power electronics with good potential for further development. The most attractive application of this technology are in the medium to high voltage range (2-13kv), and include induction motor drives, power distribution, power quality and power conditioning applications.

In general multilevel power converters can be viewed as voltage synthesizers, in which the high output voltage is synthesized from many discrete small voltage levels. The main advantages of this approach is ,The voltage capacity of the existing devices can be increased many times without the complications of static and dynamic voltage sharing that occurring series connected device. It is possible to obtain refine voltage wave forms and reduced THD in voltage with increased number of voltage levels. It is possible to reduce the electromagnetic interference problem by reducing the switching dv/dt stress. Multilevel wave forms naturally limit the problems of large voltage transients that occur due to the reflections on cables, which can damage the motor windings and cause other problems.

The diode-clamped multilevel converter employs clamping diodes and series DC capacitors to produce AC Voltage waveforms with multiple levels. The converter can be generally configured as a multilevel topology, but only the three-level converter, also referred as Multi Point Clamped (MPC) converter, has found wide application in medium-voltage high-power applications. The main features of the MPC converter include reduced *dv*/*dt* and Total Harmonic Distortion (THD) in its AC output voltages in comparison to the conventional two level converters. As in any multilevel converter it can be used in the medium-voltage applications to reach a certain voltage level without series connection of power semiconductors.
In principle, DTC method is based on instantaneous space vector theory. By optimal selection of the space voltage vectors in each sampling period, DTC achieves effective control of the electromagnetic torque and the stator flux on the basis of the errors between theirs references and estimated values. It is possible to directly control the inverter states through a switching table, in order to reduce the torque and flux errors within the desired bands limits[8][9]. The present work is based on the study of the application of DTC to the seven-level MPC VSI.

II. MULTI LEVEL DIRECT TORQUE CONTROL (MDTC)

Fig.1 shows a simple structure of the Proposed Block diagram of 7-level MPC inverter DTC IM drive. In DTC the reference to be applied is directly calculated from the equation of the load, usually an Induction Motor (IM). In the following, a short description of DTC is presented, just to introduce to its extension to multilevel VSI. Considering Park transform of IM equations, it is possible to write in equation (1), where φ_S is the stator flux, u_s, i_s and r_s are the stator voltage, current and resistance respectively.

$$\frac{d\varphi_S}{dt} = \vec{U}_S - r_S \vec{i}_S \quad (1)$$

The paper first received 27 Sep 2013 and in revised form18 Dec 2013.
Digital Ref: APEJ-2013-07-421

[1] Department of Electrical and Electronics Engineering, Vignan`s Lara Institute of Technology and Science, Vadlamudi, Guntur, India. E-mail: sekhar.obbu@gmail.com
[2] Department of Electrical and Electronics Engineering, R.V.R & J.C College of Engg, Chowdavaram, Guntur, India, E-mail: cskoritala@gmail.com.

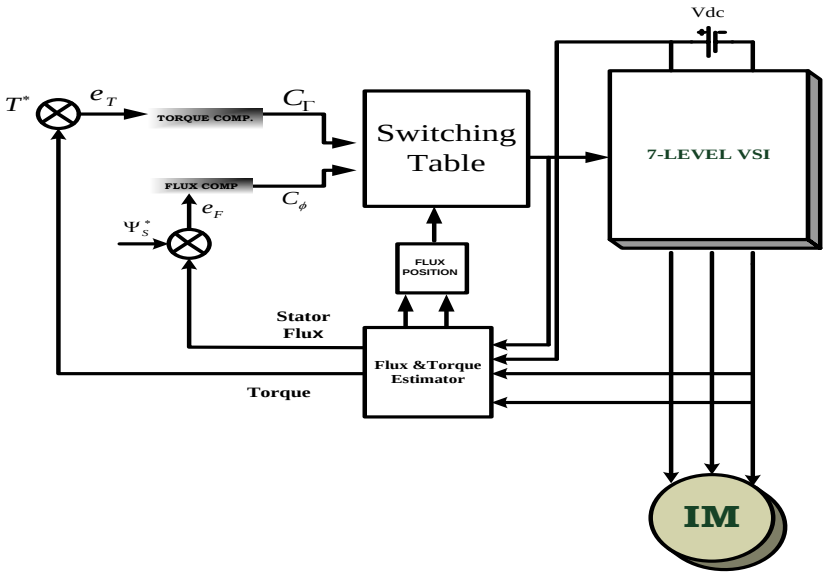


Fig.1: Proposed Block diagram of 7-level MPC inverter DTC IM drive

Ignoring the contribution of the current, which can be considered small in the respect of the stator voltage, the variation of stator flux can be ascribed all to the voltage applied. So, a proportional relationship between flux variation and voltage in a given cycle T_c can be found by discretizing (1).

$$\Delta \vec{\varphi}_S \cong T_c \vec{i}_S \qquad (2)$$

Analyzing the equation binding the stator and rotor fluxes (φ_S and φ_r) to the torque (T_e), it is possible to find that an augmentation of the angle between fluxes (ϑ_{sr}) means an augmentation of torque, as equation (3) shows, where M, σ, L_S and p are the mutual inductance, the leakage inductance and number of poles respectively.

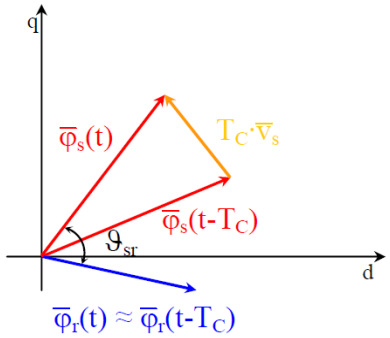


Fig.2: DTC Principles: vector representation of the stator a rotor fluxes during a sample interval T_c.

$$T_e = \frac{3}{2}\frac{p}{2}\frac{M}{\sigma L_S}\varphi_S \varphi_r \sin \nu_{sr} \qquad (3)$$

The relationship between stator and rotor fluxes it can be assumed that a fast variation of the stator flux angular speed will reflect in an increment of the angle V_{sr} as Fig.2. Schematically shows. So, imposing a particular stator voltage, it is possible to control either the stator flux amplitude or the torque. The vector $\Delta \vec{\varphi}_S \cong T_C \vec{U}_S$ can be decomposed in the component parallel and perpendicular to the stator flux; the parallel component modifies the stator flux amplitude while the perpendicular component controls the torque.

III. Seven-Level MPC VSI and Related Output Voltage Vectors

A seven-level MPC converter topology typically consists of six capacitors on the DC bus and seven levels of the phase voltage. Fig.3 shows a seven–level MPC inverter topology in which the dc bus consists of six capacitors C_1, C_2, C_3, C_4, C_5 and C_6. For a dc bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/6$, and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/6$, through clamping diodes. Each phase consists of eight switches, each one with its freewheeling diode in series and two other in parallel and two clamping diodes that allow the connection of the phases outputs to the middle point *o*. Table 1 illustrates the switching states of this inverter for one phase.

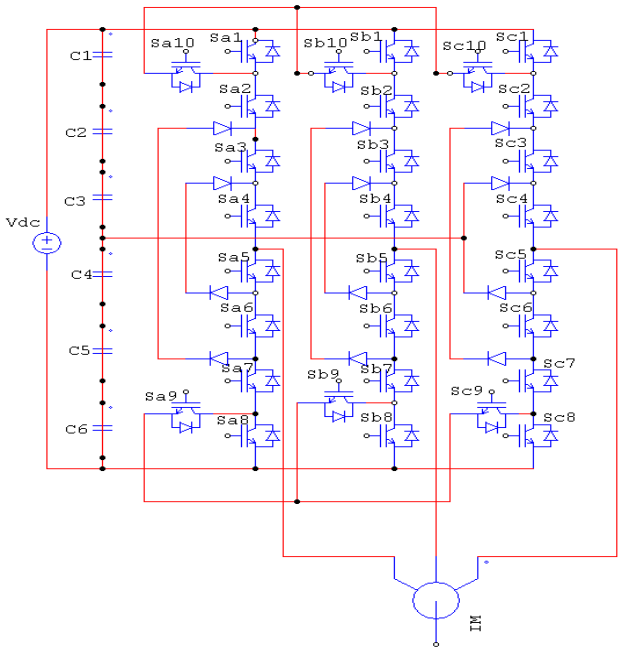


Fig.3: Seven-level MPC VSI topology

As shown in Fig.4, the number of discrete voltage vectors has increased if compared with a three-phase three-level inverter. Keeping in mind the simplicity of DTC, the same principle, as explained in [10],[11],[12] can be applied when a three-phase multilevel inverter feeds the induction machine. Having voltage vectors with different magnitudes means that different speeds of the stator-flux-linkage vector can be obtained.

Therefore, by changing the speed of the stator flux vector, the rate of change of the produced electromagnetic torque can be changed. This extra flexibility in selecting an optimal space voltage means that a more precise control of both torque and flux can be obtained. As in the three-level DTC strategy [8], [9], the α-β plane will be divided into several sectors. In a multilevel inverter the number of available discrete voltage vectors is more important than those obtained with a two or three-level inverter. Thus, the α-β plane will be divided into 12 sectors rather than six.

Table 2: Seven-level inverter output magnitudes of space voltages vectors

Group	Magnitude of Voltage Vectors
1	$[V_o]$
2	$[V_1, V_2, V_3, V_4, V_5, V_6]$
3	$[V_{44}, V_{45}, V_{46}, V_{47}, V_{48}, V_{49}]$
4	$[V_{63}, V_{64}, V_{65}, V_{66}, V_{67}, V_{68}]$
5	$[V_{75}, V_{77}, V_{79}, V_{81}, V_{83}, V_{85}]$
6	$[V_{100}, V_{101}, V_{102}, V_{103}, V_{104}, V_{105}, V_{106}, V_{108}, V_{110}, V_{112}, V_{113}, V_{114}, V_{115}, V_{116}, V_{117}, V_{118}, V_{125}]$
7	$[V_{205}, V_{206}, V_{207}, V_{208}, V_{209}, V_{210}]$
8	$[V_{218}, V_{219}, V_{220}, V_{221}, V_{222}, V_{223}, V_{224}, V_{225}, V_{226}, V_{228}, V_{230}, V_{232}, V_{234}, V_{236}, V_{237}]$
9	$[V_{296}, V_{297}, V_{298}, V_{299}, V_{300}, V_{301}, V_{302}, V_{303}, V_{304}, V_{305}, V_{306}, V_{308}, V_{310}, V_{312}, V_{314}, V_{316}]$

A seven-level inverter has 343 switching states and there are 78 effective vectors. According to the magnitude of the voltage vectors, we divide them into nine groups as shown in table2.

The flux control is made by classical two-level hysteresis controller, so a high level performance torque control is required, and the torque is controlled by a hysteresis controller built with six lower bounds and six upper known

The closed-form mathematical model of the CSI-fed induction motor drive system has been considered the bounds. A combination of the controller's outputs and the sector is then applied to a new optimal switching table

Table 3 which will give the appropriate voltage vector to reduce the number of commutation and the level of steady state ripple.

IV. Simulation and Results

Simulation studies have been carried out for the proposed inverter scheme in DTC control with qualitative space vector pulse width modulation algorithm using SIMULINK software in MATLAB environment. The induction motor parameters are as follows: Rs=4.85Ω, Rr=3.805Ω, Ls=274mH, Lr=274mH, Lm=258mH, p=2, J=31g.m2, V=220V, power=1.5kW and speed=1420rpm. All simulations have a sample time for the control loop of 100μs; the voltage of the DC bus is 514V. To show the effectiveness of the DTC with seven-level inverter with SVPWM switching technique a simulation work has been carried out on induction motor.

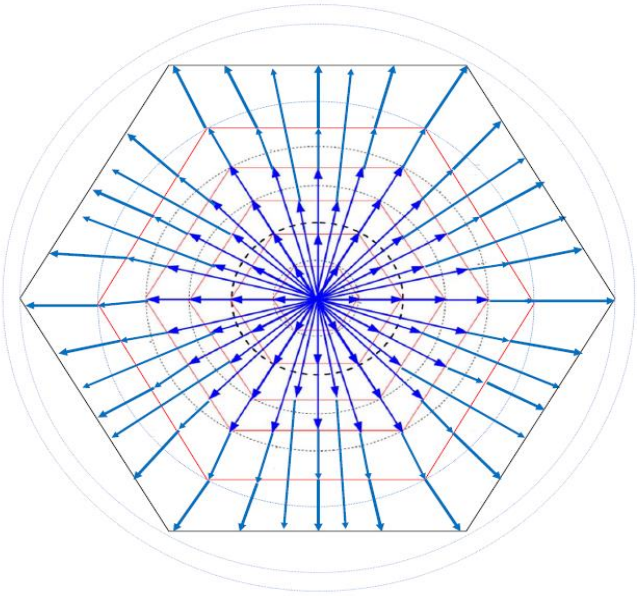
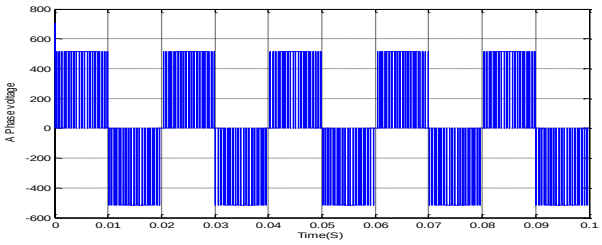
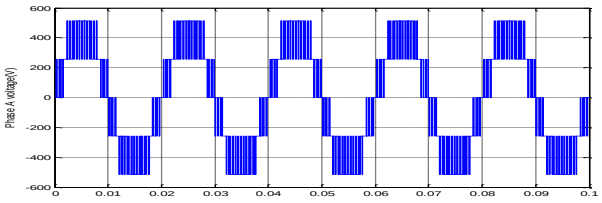


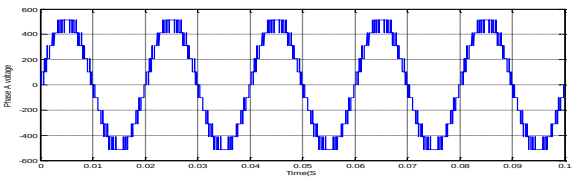
Fig.4: Space voltage vectors used in a seven-level inverter fed DTC scheme



(a)



(b)



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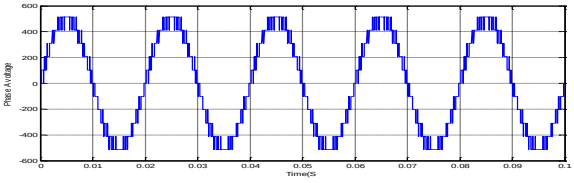
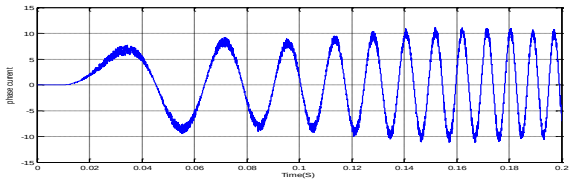
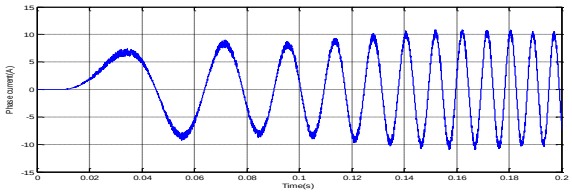


(d)

Fig.5 (a-d): Line voltage of 2, 3, 5 and 7-level inverter



(a)



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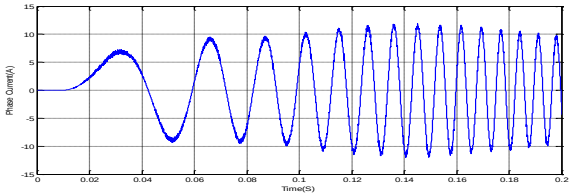

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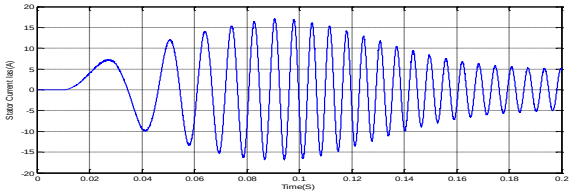
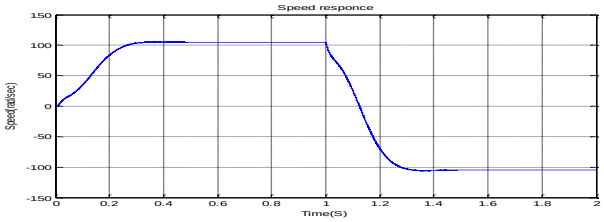
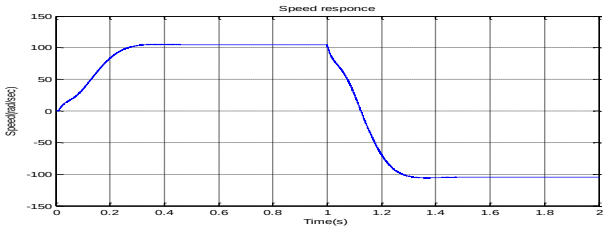


(d)

Fig.6 (a-d): Stator Phase Currents of Two-level, Three-level, Five-level and seven-level inverter fed DTC IM drive



(a)



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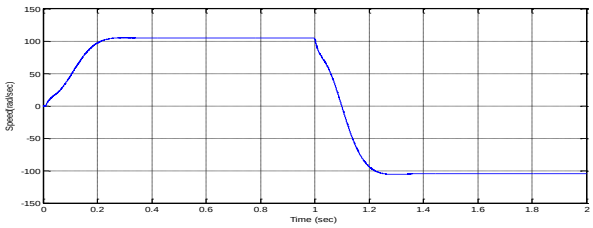

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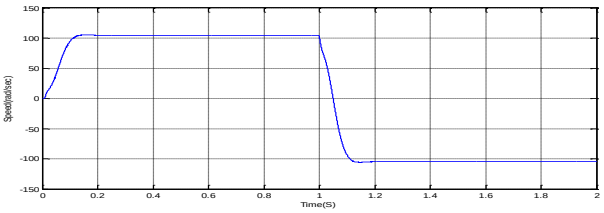
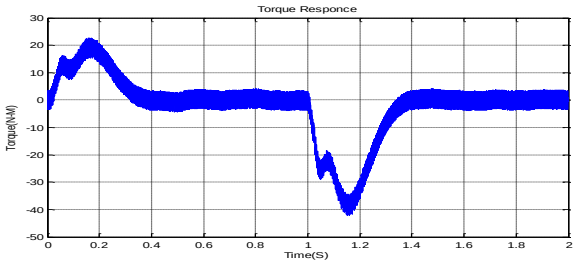
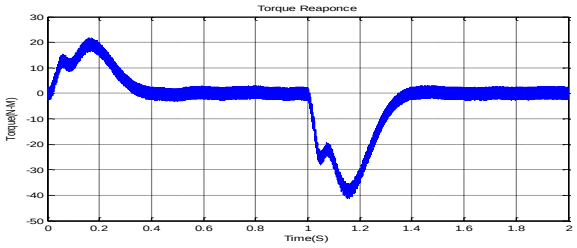


(d)

Fig.7 (a-d): Speed response of Two-level, Three-level, Five-level and Seven-level inverter fed DTC IM drive, current reversal at 1sec



(a)



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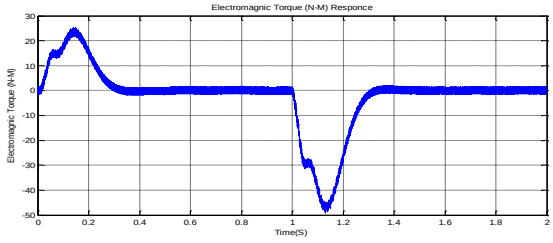

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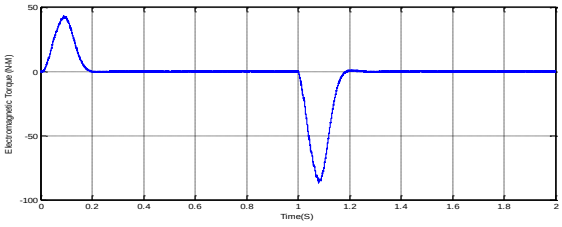

(d)

Fig.8 (a-d): Torque response of Two-level, Three-level, Five-level and Seven-level inverter fed DTC IM drive, current reversal at 1sec

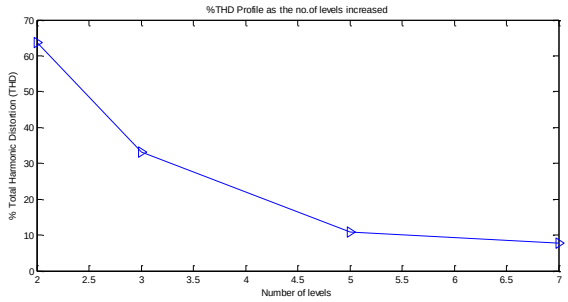

Fig.9: %THD profile as the number of levels increase

Table 1: Seven-level MPC leg relationships between configurations and output voltages

Switches state										Output Voltage (V_{AO})
S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}	S_{a9}	S_{a10}	
ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	$-3U_0$
OFF	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	OFF	$-2U_0$
OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	$-U_0$
OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	0
OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	0
OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	U_0
OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	$2U_0$
OFF	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	$3U_0$

Table 3: Proposed switching table for 7-Level MPC Inverter fed DTC IM drive

		Sectors											
C_ϕ	C_Γ	1	2	3	4	5	6	7	8	9	10	11	12
-1	-6	304	314	305	316	300	306	301	308	302	310	303	312
	-5	224	234	225	236	220	226	221	228	222	230	223	232
	-4	104	114	105	116	100	106	101	108	102	110	103	112
	-3	67	83	68	85	63	75	64	77	65	79	66	81
	-2	117	209	118	210	113	205	114	206	125	207	116	208
	-1	5	48	6	49	1	44	2	45	3	46	4	47
	0	Zero Vector											
	+1	3	46	4	47	5	48	6	49	1	44	2	45
	+2	115	207	116	208	117	209	118	210	113	205	114	206
	+3	65	79	66	81	67	83	68	85	63	75	64	77
	+4	102	110	103	112	104	114	105	116	100	106	101	108
	+5	220	228	221	230	222	232	223	234	218	224	219	226
	+6	298	306	299	308	300	310	301	312	296	302	297	304
+1	-6	300	306	301	308	302	310	303	312	304	314	305	316
	-5	226	221	228	222	230	223	232	224	234	225	236	220
	-4	101	108	102	110	103	112	104	114	105	116	100	106
	-3	77	65	79	66	81	67	83	68	85	63	75	64
	-2	207	116	208	117	209	118	210	113	205	114	206	115
	-1	48	6	49	1	44	2	45	3	46	4	47	5
	0	Zero Vector											
	+1	45	3	46	4	47	5	48	6	49	1	44	2
	+2	208	117	209	118	210	113	205	114	206	115	207	116
	+3	67	84	68	86	63	76	64	78	65	80	66	82
	+4	115	105	117	100	107	101	109	102	111	103	113	104
	+5	223	235	218	225	219	227	220	229	221	231	222	233
	+6	313	296	303	297	305	298	307	299	309	300	311	301
0	-6	305	316	300	306	301	308	302	310	303	312	304	314
	-5	225	236	220	226	221	228	222	230	223	232	224	234
	-4	105	116	100	106	101	108	102	110	103	112	104	114
	-3	68	85	63	75	64	77	65	79	66	81	67	83
	-2	210	113	205	114	206	115	207	116	208	117	209	118
	-1	49	1	44	2	45	3	46	4	47	5	48	6
	0	Zero Vector											
	+1	44	2	45	3	46	4	47	5	48	6	49	1
	+2	205	114	206	115	207	116	208	117	209	118	210	113
	+3	76	64	78	65	80	66	82	67	84	68	86	63
	+4	107	101	109	102	111	103	113	104	115	105	117	100
	+5	225	219	227	220	229	221	231	222	233	223	235	218
	+6	303	297	305	298	307	299	309	300	311	301	313	296

The stator line voltages of 2, 3, 5 and 7-level inverter system are illustrated in fig.5.In fig.6 stator current response of the 2, 3, 5 and 7-level inverters are compared. It is seen that the performance of the 7-level inverter fed DTC IM drive has lower ripple, so the proposed system is superior to control the flux with reduced ripple content. Fig.7 illustrate the speed response of 2,35 and 7-level inverter fed DTC IM drive, from simulation results proposed system has fast dynamic speed response.Fig.8 torque response of two-level, three-level, five-level and seven-level inverter fed DTC IM drive, current reversal at 1sec; demonstrates the developed DTC's achieved high dynamic performance in response to the changes in demand torque.Fig.9 shows the decrease of percentage of total harmonic distortion (%THD) in the motor line voltage as the number of levels increased (Table 4). This result in the smooth running of motor and thus the performance of the motor can be improved.

From the above discussion, the proposed DTC IM drive system behavior is optimum, even in extreme conditions like the reverse speed reference with nominal load torque applied. Reduction in ripple is observed in both electromagnetic torque and flux due to the use of hysteresis controllers.

Table 4: %THD profile as the number of level increased

Inverter	%THD
2-Level	63.78
3-Level	33.21
5-Level	10.86
7-Level	7.77

V. CONCLUSIONS

A multilevel inverter based DTC fed induction motor drive using space vector modulation is presented. The proposed DTC IM drive scheme is capable for enough degrees of freedom to control both electromagnetic torque and stator flux with very low ripple. Even with at the output voltages with extremely low distortion and lower *dv/dt*. They can operate with a lower switching frequency. As the number of levels increased the %THD in the motor line voltage decreased. As the number of levels increased the torque ripple is reduced to minimum and the stator flux ripple is also minimized. From this analysis high dynamic performance, good stability and precision are achieved.

A Seven-level inverter scheme for DTC induction motor drive is presented. The salient features of this scheme are, Results presented for a 2-level, 3-level and 5-level and 7-level inverter shows that an increase in the number of levels improves the torque quality reducing ripple amplitude. This enhancement results in a narrow torque spectrum even for high frequency harmonics. The proposed DTC IM drive system behavior is optimum, even in extreme conditions like the reverse speed reference with nominal load torque applied. From the simulation results, it can be concluded that the seven-level inverter fed DTC drive gives reduced steady state ripples and a harmonic distortion as the number of levels increased.

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BIOGRAPHIES

O. Chandra Sekhar received his B.Tech degree in Electrical & Electronics Engineering from JNTUH,India in 2005 and M.Tech with power Electronics and Electrical Drives from Vignan's Engineering College, Vadlamudi, India in 2008.He has been with Vignan's Lara Institute of Technology and Science ,Vadlamudi as Associate Professor. Presently he is a part-time research student at J.N.T.U College of Engineering, Hyderabad- 500072, India, working towards his doctoral degree. His Research interests are Power Electronics, Industrial Drives.

K. Chandra Sekhar received his B.Tech degree in Electrical & Electronics Engineering from V.R.Siddartha Engineering College, Vijayawada, India in 1991 and M.Tech with Electrical Machines & Industrial Drives from Regional Engineering College, Warangal, India in 1994. He Received the PhD degree from the J.N.T.U College of Engineering, Hyderabad, India in 2008. He is having 17 years of teaching experience. He is currently Professor and Head of Department, EEE, R.V.R & J.C.College of engineering, Guntur, India. His Research interests are Power Electronics, Industrial Drives & FACTS Devices.

Transformer-less Pulse Power Supply: A Prototype Development

S. K. Rai [1] P. Tandon [2] S. Jangid [3] R. Varma [4]

Abstract– High voltage pulse generators find extensive use in characterization and testing of high power microwave tubes and plasma devices along with many others industrial applications. The solid-state devices based method is now more popular than the pulse-forming network (PFN) based design, which is an old technique. However, both the methods entail the design of pulse transformer, which involves very critical design issues. This paper describes the prototype design and development of transformer-less pulse power supply, which is based on popular topology "Marx Generator".

Keywords– Marx Generator, pulsar, droop, isolation, PRF

I. Introduction

Today, rectangular electrical pulses of high-voltage and high-frequency have many industrial applications. Some typical applications evolve in surface treatment techniques, food sterilization, waste treatment, characterization of microwave and plasma devices etc [1-3].

Several kinds of models have been widely used for the pulse power supply such as Marx generator, hard-tube type pulse generator, Thyratron type pulse power generator with pulse forming network (PFN) etc [4-6]. The pulse width and shape of these kinds of pulse power supply are load dependent. These generators are usually designed for fixed pulse width and load.

Now days, solid-state devices based pulse generators are more popular. However, the maximum pulse width, overshoot, pulse droop and pulse shape are limited by pulse transformer design, which involves very critical design issues. The Marx Generator topology based transformer-less pulse power supply is new advancement in this. It is completely based on solid-state devices and capacitors charging and discharging [5-12].

In the past, Marx Generators were usually implemented using spark gap technology and had low pulse repetition rates [13]. In recent years, Marx generators based on semiconductor switches are proposed for high pulse repetition rates [14-15].

This paper describes the simple design and prototype development of transformer-less pulse power supply based on "Marks Generator" topology.

The paper first received 24 Dec 2012 and in revised form 22 Dec 2013.
Digital Ref: APEJ-2013-10-422

[1,3]Department of Electronics Engineering, B K Birla Institute of Engineering & Technology (BKBIET), Pilani, Rajasthan (INDIA), E-mail: satishkumarrai2000@gmail.com, jangid.santosh@gmail.com
[2]Electronics and communication Engineering, COER, Roorkee, Uttarakhand (INDIA), E-mail: prakhar.tandon1989@gmail.com
[4]Cheif Scientist & Group Leader, Industrial Electronics Group, CSIR-CEERI, Pilani, Rajasthan (INDIA), E-mail: rv@ceeri.ernet.in

The design calculation is done for Input Voltage = 800V, Output voltage up to 15kV, f_s = up to10kHz, Pulse Width up to 5µs, Droop = 10% and Maximum Pulse Current = 1A.

A combination of 20 modules with suitable gate drivers is used in this application.

II. System Description and Design

The schematic diagram of proposed pulsar is shown in Fig. 1. Incoming single-phase ac supply is rectified and filtered after step-up using transformer and the output dc is controlled by using a variac. The available output dc voltage charges the capacitors (C_1 to C_{20}) using IGBTs (Q_1 to Q_{20}) for specified time and after some delay IGBTs (Q_{21} to Q_{40}) connects all the capacitors in series and so produces the required high pulse to the connected load. Diodes (D_1 to D_{40}) are used to provide unidirectional current flow in both charging and discharging of capacitors.

This system has twenty sub-modules as per design. A single sub-module is shown with the dotted rectangular box (Fig. 1).

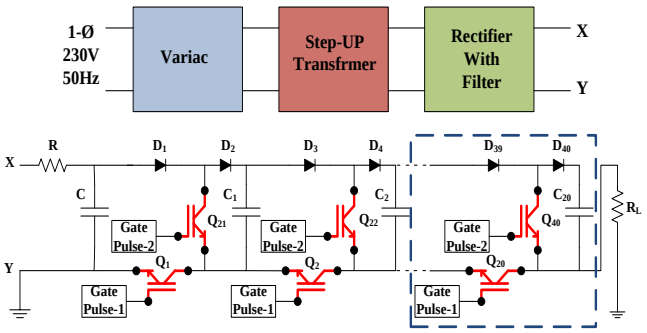

Fig. 1: Schematic diagram of proposed pulsar

The schematic diagram of developed prototype is shown in Fig. 2. Only three sub-modules are tested and an isolation transformer is used for isolation purpose at input side.

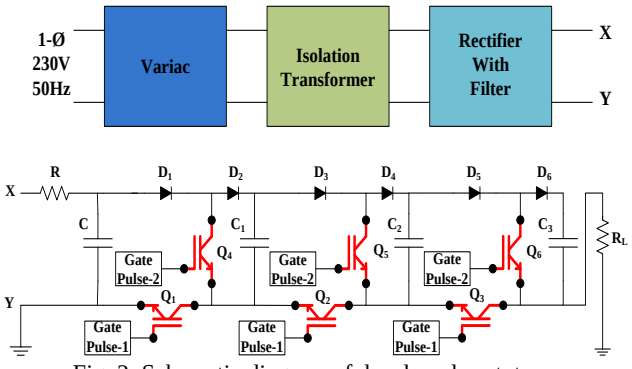

Fig. 2: Schematic diagram of developed prototype

The working of the prototype can be understood by capacitors charging schematic diagram (Fig. 3) and discharging schematic diagram (Fig. 4). Initially, when gate pulse-1 is applied to IGBTs (Q_1 to Q_3), all the capacitors (C_1 to C_3) are connected in parallel fashion to the DC voltage source and charged fully (Fig. 3). During this period load is connected to ground via IGBTs and so the output voltage is about zero. After charging, gate pulse-2 is applied with some delay to the IGBTs (Q_4-Q_5), all the capacitors are connected in series and the voltage (V_c+V_{c1}+V_{c2}) is appeared across the connected load (Fig. 4). During series connection, capacitors discharge and in the next cycle again these are charged fully and so on. All the diodes are forward biased during charging time but during discharging only odd numbered diodes (D_1, D_3 & D_5) work, rest of the diodes (Even numbered: D_2, D_4 & D_6) are in reverse biased mode and prevent capacitor discharge by short circuit.

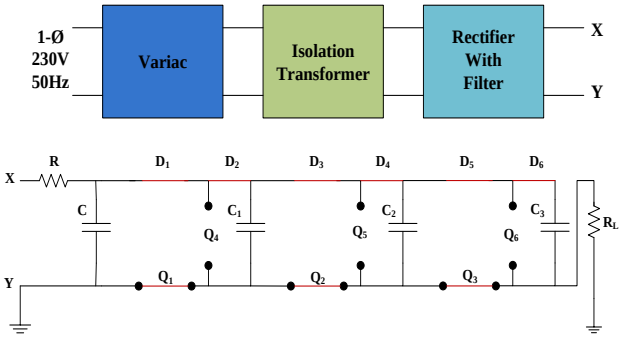

Fig. 3: Schematic diagram of capacitors charging

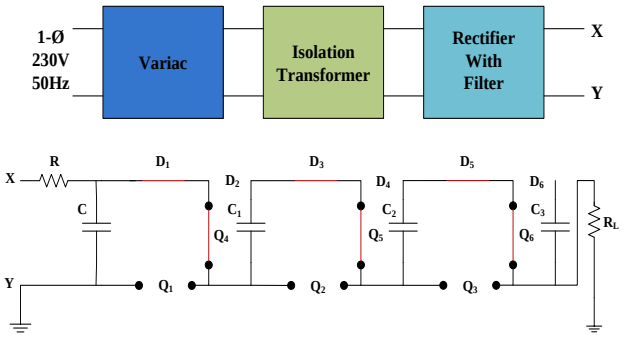

Fig. 4: Schematic diagram of capacitors discharging

Each IGBT has its own isolated gate pulse and gate drive supply. The gate pulses are applied using fiber optic. The gate pulse width of charging IGBTs is fixed but for series connecting IGBTs, it is variable and so the output pulse varies accordingly. The prototype is tested with resistive load. Moreover, no pulse transformer is required in this approach. Details of design calculation and construction of sub-systems are discussed in the following sub sections.

A. Design Calculations

Design Specifications:

Input Voltage: up to $800V$
Output Voltage: up to $15kV$
Pulse width: up to $5\mu s$
Pulse Frequency: up to $10kHz$
Droop: 10%
Maximum pulse current: $1A$

$$No.of\ Modules = \frac{MaxoutputVoltage}{MaxInputVoltage} = \frac{15kV}{800V} = 18.75$$

$$C_{equ.} = \frac{MaxPulseCurrent \times MaxPulseWidth}{Droop} = \frac{1A \times 5\mu s}{10\%of\,15kV} = 3.3nF$$

$$SingleCapacitorValue = C_{equ.} \times (No.ofModules + 1)$$
$$= 3.3nF \times 21 = 69.3nF$$

$$CapacitorVoltageRating \succ MaxInputDCvoltage(800V)$$

$$PeakDiodeCurrent \succ \frac{MaxInputDCvoltage}{R = 50\Omega} = \frac{800V}{50\Omega} = 16A$$

$$AverageDiodeCurrent \succ$$
$$PeakDiodeCurrent \times MaxPulsewidth \times MaxFrequency$$
$$= 16A \times 5\mu s \times 10kHz = 0.8A$$

$$PeakInverseVoltageof\ Diode \succ MaxInputDCvoltage = 800V$$

$$Max(V_{CE})of\ IGBT \succ MaxCapacitorvoltage = 800V$$

So twenty modules are decided as per above calculation with resistance R=50Ω, which is decided as per the required charging time of the capacitor. All the capacitors (C & C_1 to C_{20}), all diodes and all IGBTs are selected 1 µF/2kV, 6FMLR120 (6A/1200V) and IXGH15N120CD1 (30A/1200V) respectively with the reference of above calculations. The fixed gate pulse width of 80 µs is decided for charging IGBTs.

B. Gate Pulse Generator

The optical coupling based open loop gate pulse generator has been designed to trigger the IGBTs [16].

Gate Pulse Generator Specifications:

Pulse Frequency: up to 10kHz
Pulse-1 (for charging IGBTs): 80 µs (Fixed)
Pulse-2 (for series Connecting IGBTs): up to 5 µs
Delay (Pulse-1 to Pulse-2): 10 µs (Fixed)

The above specified gate pulses details are generated using the concept as shown in Fig. 5 and realized by using NE555 and 4047BP as shown in Fig. 6, which has both pulse width and frequency control facilities. The generated gate pulses are transmitted optically by using transmitter HFBR1521. Since, same pulse is required by several IGBTs, so ULN2003 (Seven Darlington Array) is used with transmitters. The pulse generator system is shown in Fig. 7.

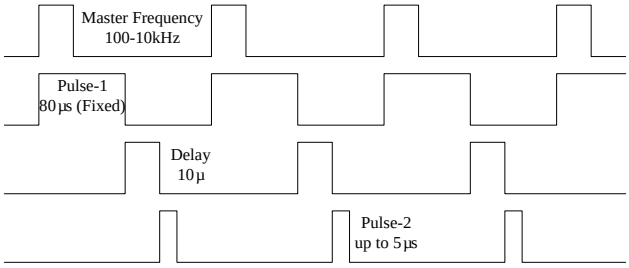

Fig. 5: Followed concept to generate of gate pulses

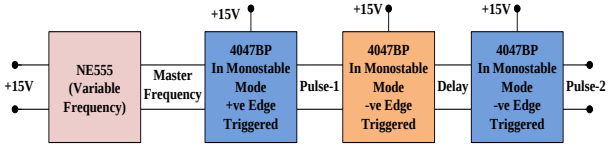

Fig. 6: Block diagram of pulse generator

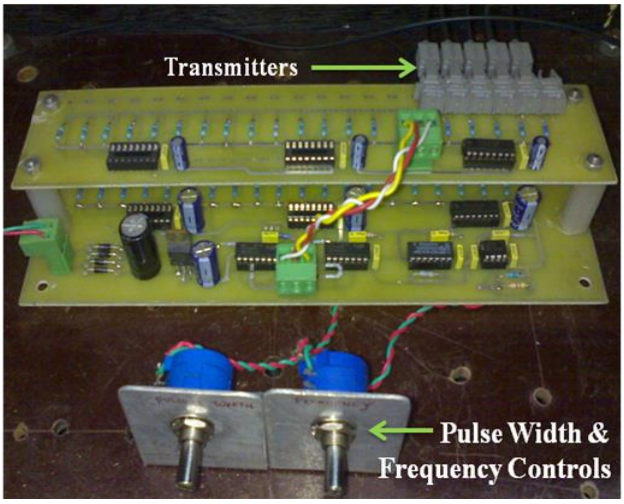

Fig. 7: Pulse generator system

C. Isolated Gate Driver

The required floating gate drive supply for all IGBTs is realized with simple arrangement as shown in Fig. 8 [16]. A high voltage insulated wire acts as primary of the transformer, which passes through the ferrite ring core behaving as secondary. It is driven by low voltage high frequency inverter (15V, 20kHz). The induced voltage in the secondary is rectified, filtered and regulated to generate isolated gate drive supply for each IGBT. The optically transmitted gate pulse is received and transferred into the electrical pulse using optical receiver HFBR2521. The gate driver IXDD414CI is used for fast switching of IGBTs. The inverter system, gate driver system with optical receiver, gate driver power supply and received gate pulses waveform are shown in Fig. 9, 10, 11, 12 and 13 respectively.

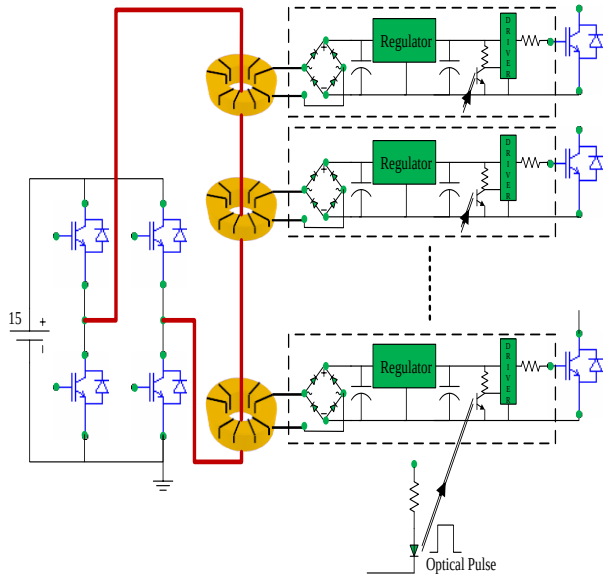

Fig. 8: Schematic diagram of floating gate drive supplies and controls

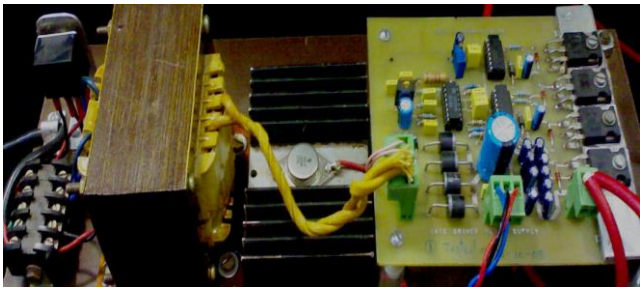

Fig. 9: Inverter of gate drive supplies

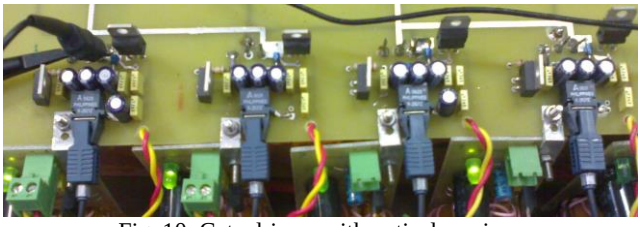

Fig. 10: Gate drivers with optical receiver

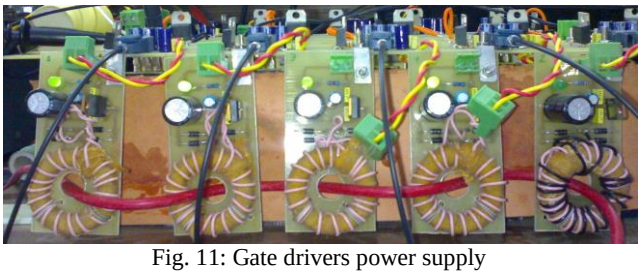

Fig. 11: Gate drivers power supply

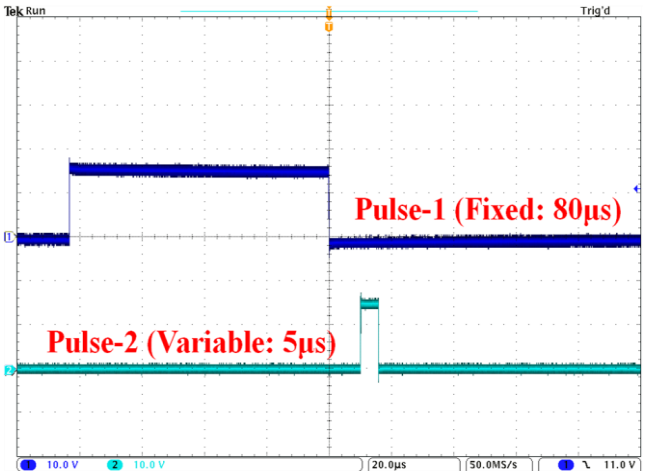

Fig. 12: Received gate pulses (Both waveforms: 10V/div, 20µs/div)

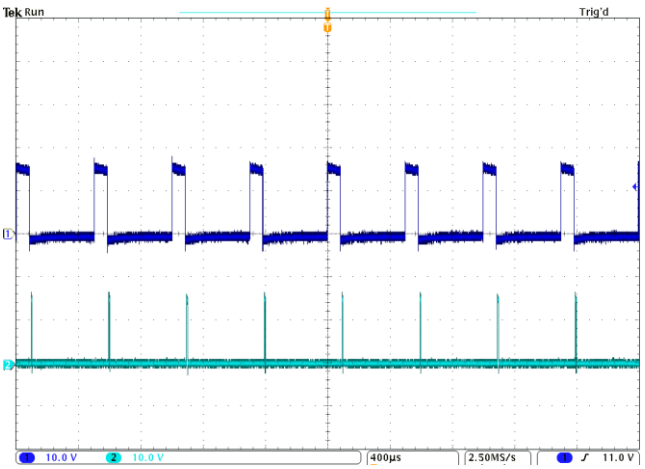

Fig. 13: Received gate pulses [Multiple Pulses- Upper: Pulse-1, Lower: Pulse-2 (Both waveforms: 10V/div, 400µs/div)]

III. Test Result

Presently, the prototype is tested with only three modules as shown in Fig. 2 but design calculations are considered for twenty modules as shown in Fig. 1.

The test results are shown for the input DC voltage of 200V and output voltage is obtained 600V, which is as per the design. The developed prototype is tested successfully with resistive load for maximum rated pulse current at 600V pulse voltage, over the entire range of the pulse width and pulse repetition frequency (PRF).

The rise time of the output pulse is found about 30ns. However, the induced noise at the gate of the charging IGBTs at switching time of series connecting IGBTs is an issue to be rectified.

The test setup, developed prototype, top view of prototype and different waveforms are shown in the figures given below.

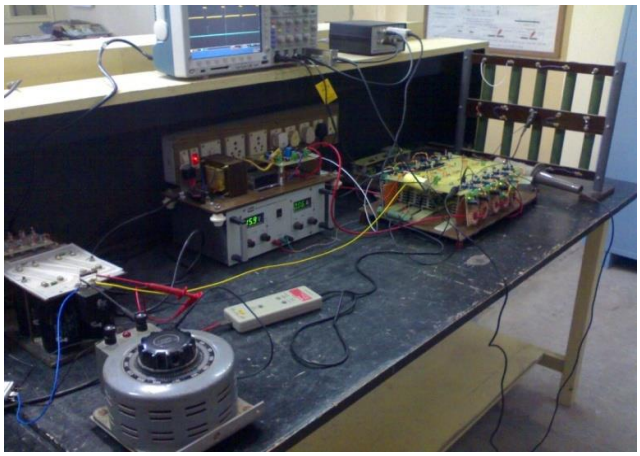

Fig. 14: Test setup

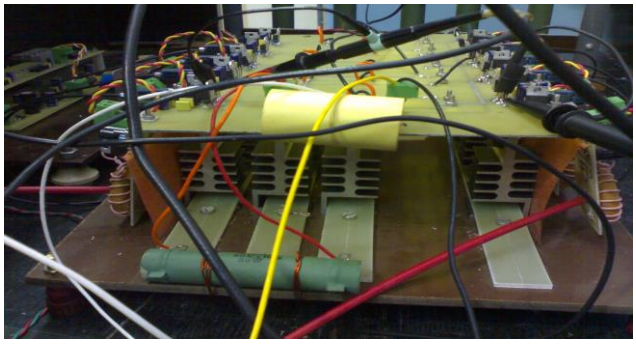

Fig. 15: Developed prototype

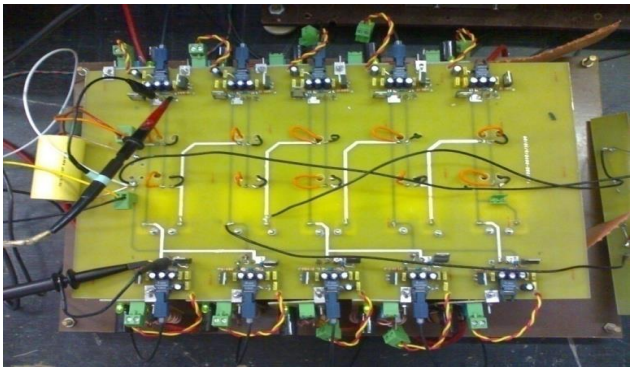

Fig. 16: Top view of developed prototype

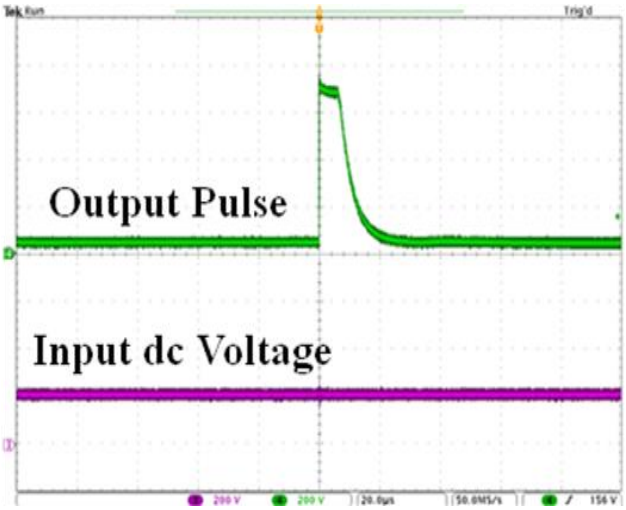

Fig. 17: Output pulse with input dc voltage (Both waveforms: 200V/div, 20µs/div)

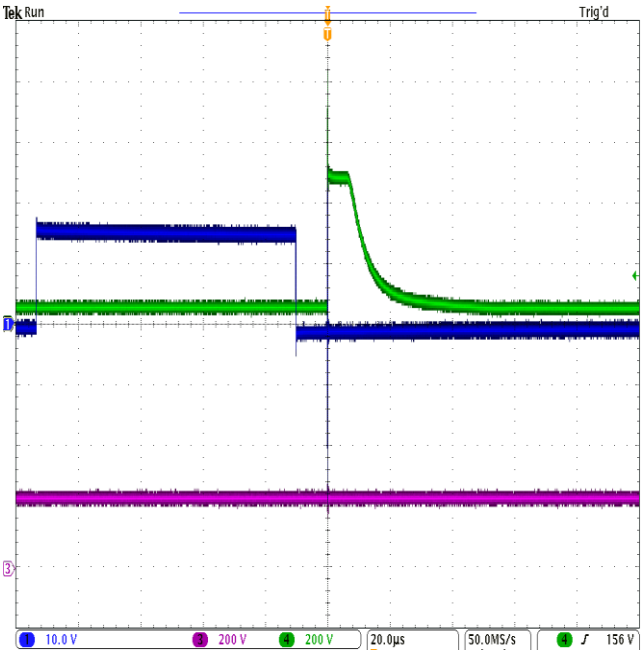

Fig. 18: Output pulse (Upper) with input dc voltage (Lower) and gate pulse-1 (Middle) (Both waveforms: 200V/div, 20µs/div)

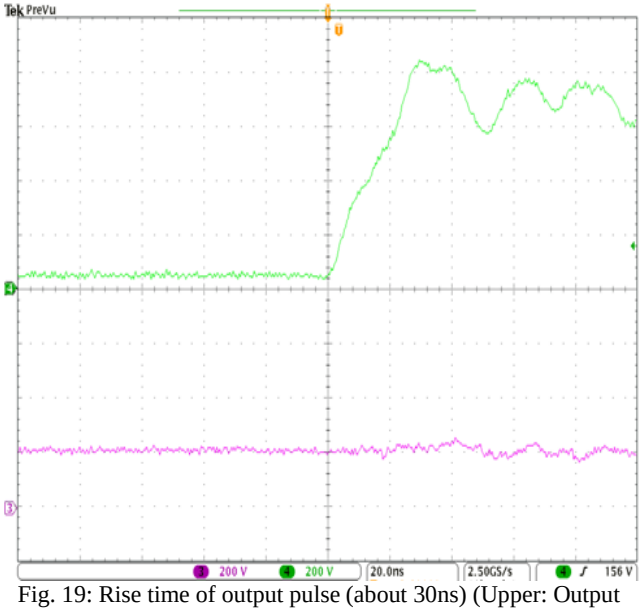

Fig. 19: Rise time of output pulse (about 30ns) (Upper: Output Pulse, Lower: Input DC voltage, Both waveforms: 200V/div, 20ns/div)

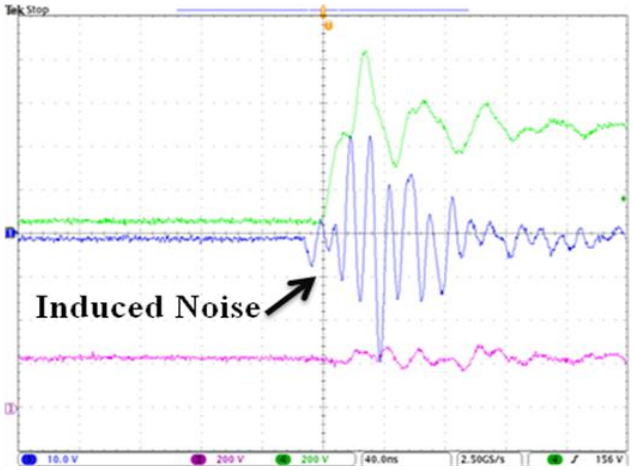

Fig. 20: Induced noise at the gate of charging IGBT (Upper: Output Pulse, Middle: Induced Noise, Lower: Input DC voltage, Upper & Lower waveforms: 200V/div, 40ns/div, Middle waveform: 10V/div, 40ns/div)

IV. Conclusion

In this paper, the design and development of the prototype of transformer-less pulse power supply based on "Marx Generator" are described. The design calculations are done for the following specification:

Input Voltage: up to 800V
Output Voltage: up to 15kV
Pulse width: up to 5 μs
Pulse Frequency: up to 10kHz
Droop: 10%
Maximum pulse current: 1A

The optical coupling based open loop gate pulse generator has been designed to trigger the IGBTs, which has following specifications:

Pulse Frequency: up to 10kHz
Pulse-1 (for charging IGBTs): 80 μs (Fixed)
Pulse-2 (for series Connecting IGBTs): up to 5 μs
Delay (Pulse-1 to Pulse-2): 10 μs (Fixed)

As per the design, twenty modules have been selected to achieve required output. The test results for the prototype with three modules have been presented and are found as per design and requirement.

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Acknowledgment

The authors would like to thank CSIR-CEERI, Pilani and B K Birla Institute of Engineering & Technology (BKBIET), Pilani for supporting this work.

Biographies

S. K. Rai was born in Rupanchak, Bihar, India in 1985. He received the B.Tech degree in Electronics & Communication Engineering from The ICFAI University, Dehradun, Uttrakhand, India in 2008. From 2008-2010, he worked as Project Assistant at Central Electronics Engineering Research Institute (CEERI), Pilani, India in the field of Pulse Power Supply Development. He is currently with B K Birla Institute of Engineering and Technology (BKBIET), Pilani, India as Assistant Professor. His current research interest focus on high voltage pulsed power supply, power supply development, high power pseudospark switch, gas discharge application and digital controller design.

P. Tandon was born in Moradabad, Uttar Pradesh, India in 1989. He received his B.Tech degree in Electronics and Telecommunication Engineering from College of Engineering Roorkee (Uttrakhand), India in 2011. He is pursuing M.Tech in VLSI Design at Malaviya National Institute of Technology (MNIT), Jaipur, India. His current research interests focus on VLSI, DSP and analog and digital control design.

S. Jangid was born in Pilani, Rajasthan in 1977. He received the AMIETE degree in Electronics & Communication Engineering from Institution of Electronics & Communication Engineering (New Delhi) in 2001. He was Lecturer in Polytechnique BTTI, Pilani from Year 2002 to 2007 & designated as Sr. Lecturer in BTTI in the department of Electronics & Communication in July 2007. He obtained his M.Tech (Digital Communication) from RTU in April 2011 & designated as Assistant Professor in B K Birla Institute of Engineering and Technology Pilani, in the department of Electronics & Communication. His current research interests focus on devices, circuits & communication.

Rahul Varma was born in Madhya Pradesh, India in 1953. He received the BE degree in Electronics Engineering from Maulana Azad College of Technology Bhopal, Madhya Pradesh (currently known as Maulana Azad National Institute of Technology Bhopal), INDIA and MS degree from Indian Institute of Technology (IIT), Madras, INDIA. He is working as a scientist in Central Electronics Engineering Research Institute (CEERI), Pilani, India since 1977. Presently, he is chief scientist and group leader of Industrial Electronics Group (IEG), CSIR-CEERI, Pilani. His current research interests focus on motor drives, high voltage pulsars and power supplies. He has published a number of papers in international and national reputed journals including IEEE, IET etc.

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